Using Statistical Student's *t*-Test to Qualify the Electrical Performance of the Diamond MOSFETs

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***Abstract*— This study describes the use of the Student's t-Test to qualify statistically the impact of using the Diamond (hexagonal) layout style in the electrical performance of Silicon-On-Insulator (SOI) MOSFETs. A sample of 360 SOI Metal-Oxide-Semiconductor Field Effect Transistors, n-type (nMOSFETs) were used to perform this experimental work. Regarding the SOI MOSFETs saturation drain current (I_{DSsat}), the results of this study indicate that the Diamond SOI nMOSFETs for all considered angles present higher I_{DSsat} mean values in comparison to those measured from the standard rectangular SOI MOSFET counterparts, considering that they present the same gate areas, channel width and bias conditions (with a bias condition of 1V between the drain and source and a bias condition of 0.4V between the gate and source). For all the other α angle, that is, 36.9°, 53.1°, 90.0°, 126.9° and 143.1°, the DSnM I_{DSsat}/(W/L) mean value is higher than the CSnM I_{DSsat}/(W/L) mean value in an order of 51.3%, 37.6%, 40.9%, 19.0% and 10.6%, respectively. Therefore, this statistical approach can be used as a power statistical tool to validate electrical parameters and figures of merit of devices and integrated circuits regarding the nanoelectronics area.**

Keywords: Diamond MOSFET, hexagonal layout style, SOI nMOSFETs, statistical Student's *t*-Test, statistical qualification.

I. INTRODUCTION

The continuous improvement (new structures, materials, manufacturing processes, innovative layouts, downscaling, etc.) of the Silicon-On-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) technologies enormously affects the electrical performance of Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (FETs) [1-8]. Newly, some pioneering layout styles for MOSFETs were proposed which use the "Interface Engineering between the Drain/Source and Gate Regions", or simply "gate layout changing of MOSFETs" to boost the electrical performance of the SOI Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). This layout approach is not still commercially explored by the semiconductor and ICs industries and it does not add any extra cost to the current and sophisticated CMOS ICs manufacturing processes, such as the Bulk, SOI, Ultra-Thin Body SOI FETs (UTB), Ultra-thin body and buried oxide (UTBB), Tunnel FET, etc.) [9,10]. In this scenario, the Diamond (hexagonal gate geometry) layout style for SOI MOSFETs is an example of this layout approach, according to Fig. 1, which illustrates an example of a layout of a Diamond SOI MOSFET, n channel (DSnM).

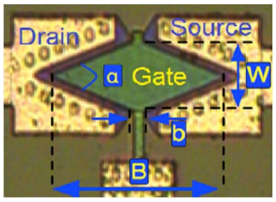

Fig. 1. Example of a DSnM.

In Fig. 1, the b and B are the smallest and highest dimensions concerning the channel length of the DSnM and α is the angle defined by the metallurgical pn junctions of the drain/silicon film (channel)/source regions, and W is the channel width. The hexagonal gate shape for SOI MOSFETs causes two new electrical effects in the SOI MOSFETs structure: I- the Longitudinal Corner Effect (LCE) that is responsible for increasing the resultant longitudinal electric field (RLEF) along its channel of SOI MOSFET in comparison to the one measured in the conventional (rectangular) SOI MOSFET (CSM), considering that they have the same W, gate area (A_G), and bias conditions [9-11]; II- The PArallel connection of MOSFETs with Different Channel Lengths (b≤L≤B) Effect (PAMDLE) which is able to reduce the effective channel length [L_{eff}=(B-b)/ln(B/b)] of the Diamond SOI MOSFET (DSM) in relation to the one found in the CSM counterpart (same W and A_G), due to the drain current (I_{DS}) of the DSM tends to further flow by its edges [9-11]. It is important to highlight that the channel length (L) of a CSM must be equal to (b+B)/2 to present the same W and A_G of a DSM counterpart. Both effects happen simultaneously in the DSM and they are responsible for boosting its main analog and digital electrical parameters and figures of merit in relation to the one found in the CSM counterpart, considering they present the same W, A_G, and bias conditions.

Nowadays, the use of statistical tools to guarantee the effectiveness of a specific product is widely used in different

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areas of human knowledge, mainly those related to the vaccines (medicine area) and quality control of the services offered by the clinical laboratories. As for instance, the Student's t-test has been utilized to test the proliferative response on the T-clones to study the effectiveness of the vaccination against autoimmune mouse diabetes with a T-cell [12]. Another application of the Student's t-test was regarded in the internal quality control of a clinical laboratory in order to verify the effectiveness of its different chemical and electrical test systems [13]. Besides, the Student's t-test was also applied to statistically study if the Brazilian companies (supply, production, and customer relations) value the time-based management at strategic and operational levels and if they reach higher profits than those that use other types of management [14]. In this scenario, this paper describes the use of the Student's t-test to statistically qualify the electrical performance of the Diamond (hexagonal gate shape) layout style for MOSFETs in relation to those found in the conventional (rectangular gate geometry) MOSFET counterparts. Besides, to show that this simple approach can be used in the microelectronics area, mainly to statistically validate the electrical performance of new devices and CMOS ICs technologies.

II. Statistical analysis

The main application of a statistical test considering the electrical parameters of a device that are obtained by experimental data is to verify statistically whether the mean values of a specific parameter obtained from two or more different samples are statistically different, higher or smaller than each other. Therefore, we can use the Student's t-test to verify if the mean values of the DSnMs $I_{DSsat}/(W/L)$, due to the LCE and PAMDLE effects, are statistically higher than those measured of the CSnM counterparts. Besides this approach can be extended for all electrical parameters and figures of merit of DSnMs to statistically qualify their electrical performance in relation to the CSnM counterparts [15,16].

For the application of this statistical test, it is necessary to create a hypothesis [15,16]. The affirmative hypothesis (or the null hypothesis, H_0) states that the means of the studied electrical parameter of the two samples (DSnMs and their CSnMs counterparts) are statistically equivalent [15,16]. The other hypothesis, that is, the alternative hypothesis (H_A) states that there are statistical differences between the means of the studied parameter of the two samples, or that one mean value is higher than the other mean values, as a function of a confidence level. The Student's t-test consists of the determination of the value of t, given by equation (2) [15,16].

$$t = \frac{\bar{x}-\mu}{\frac{s}{\sqrt{n'}}} \quad (2)$$

where in equation (2), $\bar{x}$ is the general mean value of the different measured values of a given parameter to be studied regarding different samples, μ is an individual value measured of a parameter of one of the samples, which is to be compared to the $\bar{x}$ value, and s is the standard deviation of the considered sample [15,16]. In order to accept or reject the H_0, it is possible to proceed in two different ways: I) determination of a value named "critical t"; II) by comparing the p value with the significance level [15,16]. The calculation of the value of the "critical t" allows to create the acceptance and rejection intervals of the hypotheses chosen for the Student's t-test, that is, if the value of t calculated through equation (2) is within the acceptance interval, therefore we consider the H_0 to be true, otherwise the H_0 will be considered false [12,13]. This value of the "critical t" is defined through the use of a Student's t-test table, which is defined by the number of degrees of freedom (df) and also by the level of significance (α ') [15,16]. The other way of accepting or rejecting of the H_0 is by comparing the p value with the significance level [15,16]. This value of p is the area under the distribution curve of the t-Student's t-test of the rejection regions of H_0 [15,16]. Thus, if the value of p is greater than the value of the level of significance (α ') chosen, we must consider the H_0 true, if the value of p is lower than the value of the level of significance (α'), the H_0 should be considered false [15,16]. The statistical software named Minitab 2018 was used to perform this work.

III. Description of the devices

The DSnMs and their n-type Conventional SOI MOSFET (CSnM) counterparts were manufactured by using a 1 μm SOI CMOS manufacturing process from *Université catholique de Louvain* (ICTEAM/ELEN, UCL, Belgium). The Keithley 4200 was used to perform the electrical characterizations of the devices. The main technological parameters of the fully depleted SOI nMOSFETs are: the gate oxide (t_{ox}), silicon film (t_{SI}), and buried oxide (t_{BOX}), whose thicknesses are respectively 30 nm, and 80 nm, 390 nm. The doping concentrations of the drain/source and channel are equal to $4x10^{20}$ cm^{-3} and $6x10^{16}$ cm^{-3}, respectively. This study considers 9 CMOS SOI ICs, investigating 40 transistors from each of the integrated circuits. The 40 SOI nMOSFETs studied are composed by 4 sets of 5 pairs of SOI nMOSFETs (DSnM and CSnM counterparts), regarding the same W (12 μm, 24 μm, 30 μm and 180 μm, respectively), same A_G, and with different values of α angles (36.9˚, 53.1˚, 90˚, 126.9˚, and 143.1˚, respectively). This totalizes an amount of 360 transistors considered in this work. The threshold voltage (V_{TH}) of these devices is practically the same (0.4 V). Table I presents the dimensions of the devices under investigation.

Table I. Dimensions of the devices under investigation.

General Parameters								DSnM												CSnM			
A_G (μm)				W (μm)				α(°)	b(μm)			B (μm)				L_{eff} (μm)				L_{eff} (μm)			
240	960	1500	54000	12	24	30	180	36.9	2	4	5	30	38	76	95	570	12.3	24.6	30.8	184.5	20	40	50	300
168	672	1050	37800	12	24	30	180	53.1	2	4	5	30	26	52	65	390	9.39	18.8	23.5	140.9	14	28	25	210
96	384	600	21600	12	24	30	180	90.0	2	4	5	30	14	28	35	210	6.17	12.3	15.4	92.6	8	1	20	120
60	240	375	13500	12	24	30	180	126.9	2	4	5	30	8	16	20	120	4.33	8.66	10.8	64.9	5	10	12.5	75
48	192	300	10800	12	24	30	180	143.1	2	4	5	30	6	12	15	90	3.64	7.29	9.11	54.6	4	8	10	60

IV. STATISTICAL ANALYSIS

The Student's t-test have considered the characteristic curves [I_{DS} as a function of the drain voltage (V_{DS})] of the 360 SOI MOSFETs to take into account their saturation drains currents (I_{DSsat}). The test used to verify if the data samples have a normal distribution is the Anderson – Darling test. The level of significance chosen for the application of this test is 0.005 (which means that this statistical test will be performed with a precision of accuracy equal to 99.5 %) [15, 16]. All the results indicate that the samples used to perform this paper have a normal distribution, therefore, this result allows to apply the Student's t test. The Student's t-test was applied considering the mean values of the $I_{DSsat}/(W/L)$ of the DSnMs and their CSnM counterparts, aiming to verify if the mean values of the $I_{DSsat}/(W/L)$ of the DSnMs are statistically higher than those of the CSnM. To perform this study, we create two hypotheses that will be responsible for comparing the mean values of the $I_{DSsat}/(W/L)$ of the DSnMs and CSnM counterparts. Table II illustrates the hypotheses for the application of the Student's t-test.

Table II. Hypotheses created for the application of the Student's t-test to verify if the mean values of the DSnMs $I_{DSsat}/(W/L)$, regarding each angle α, are higher than those found in the CSnM counterparts.

Hypothesis 1	**DSnM - 143.1°**		**CSnM counterpart**
H_0 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	=	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
H_1 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	>	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
Hypothesis 2	**DSnM - 126.9°**		**CSnM counterpart**
H_0 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	=	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
H_1 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	>	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
Hypothesis 3	**DSnM - 90.0°**		**CSnM counterpart**
H_0 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	=	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
H_1 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	>	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
Hypothesis 3	**DSnM - 53.1°**		**CSnM counterpart**
H_0 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	=	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
H_1 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	>	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
Hypothesis 4	**DSnM - 36.9°**		**CSnM counterpart**
H_0 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	=	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$
H_1 :	$\bar{\mu}_{I_{DSsat}/(W/L)} - DSnM$	>	$\bar{\mu}_{I_{DSsat}/(W/L)} - CSnM$

Table III illustrates the p values obtained through the application of the Student's t-test taking into account the $I_{DSsat}/(W/L)$ mean values that were experimentally obtained of the DSnMs and CSnM counterparts. The significance level considered for this study was of 0.05. In this way, the level of significance indicates the percentage of certainty in which the Student's t-test is applied, that is, if the level of significance is equal to 5%, it means that the Student's t-test will be performed with an accuracy of 95% [15, 16].

Table III. The p values resulting from the application of the Student's t-test taking into account the $I_{DSsat}/(W/L)$ mean values of the DSnMs and CSnM counterparts (experimental data).

α (°)	p
36.9	0.000
53.1	0.000
90.0	0.000
126.9	0.000
143.1	0.001

By analyzing the results of Table III, we observe that the values of p are always smaller than the value of the chosen significance level, which in this case was of 0.05. Therefore, we can conclude that all the null hypotheses illustrated in Table II were rejected, that is, the $I_{DSsat}/(W/L)$ mean values, for all the α angles, of the DSnMs are statistically higher than those experimentally measured of the CSnM counterparts, regarding a confidence level of 95%. Thus, for all the analyzed α angles, the DSnMs $I_{DSsat}/(W/L)$ mean values are statistically higher than those obtained of the CSnM counterparts. This can be justified due the existence of the LCE and PAMDLE effects in the Diamond SOI nMOSFETs. Besides, Fig.2 illustrates the mean values of the DSnMs $I_{DSsat}/(W/L)$ and those measured of the CSnM counterparts, regarding all the α angles considered in this work.

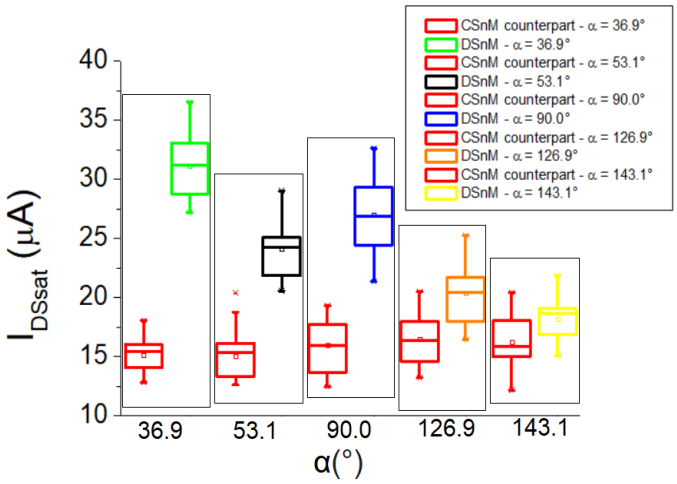

Fig. 2. The mean values of the DSnMs $I_{DSsat}/(W/L)$ and those found in the CSnMs counterparts as a function of the DSnMs α angles studied.

Analyzing Fig.2, we observe that as the α angle of the DSnM is reduced, the mean value of the DSnM $I_{DSsat}/(W/L)$ increases and it becomes further higher than the one measured in the CSnM counterpart. This can be explained due to the LCE

(higher interaction between the vectorial components of the longitudinal electric field in the channel region) and PAMDLE (smaller DSnMs L_{eff} in relation to the L of the CSnM counterparts due to the DSnM I_{DS} tends to further flow in its edges as a consequence of the B is further higher than b) effects further becomes more effective as the α angle of the DSnM is reduced. Besides, regarding the α angle equal to 36.9°, the mean value of the DSnM I_{DSsat}/(W/L) is remarkably 51.3% higher than the one measured in the CSnM. Furthermore, for the other α angles, that is, 53.1°, 90.0°, 126.9° and 143.1°, the mean value of the DSnM I_{DSsat}/(W/L) are 37.6%, 40.9%, 19.0% and 10.6%, respectively, higher than those obtained of the CSnM counterparts. Therefore, by using the Student's t-test, it is possible to affirm that for all the α angles of the DSnMs considered in this work, the mean values of their I_{DSsat}/(W/L) are statistically higher than those measured of the CSnM counterparts, regarding the same W, A_G and bias condition.

V. CONCLUSIONS

This study uses the Student's t-test to statistically prove the better electrical performance of the Diamond (hexagonal gate shape) SOI nMOSFETs in relation to that found in the CSnM counterparts (sample of 360 transistors). The experimentally obtained results indicate, for all the α angles considered in this study, that the mean value of the DSnM I_{DSsat}/(W/L) is always statistically higher than those observed in the CSnM counterparts, mainly because of the LCE and PAMDLE effects, in the best case of 51.3% for the α angle of 36.9°. Besides, this study guarantees the presence of the LCE and PAMDLE effects in the SOI MOSFETs, regarding different α angles and on the SOI CMOS ICs manufacture process. Therefore, the Diamond (hexagonal gate geometry) layout style can be considered a low-cost and simple way to enhance the electrical performance of the SOI MOSFETs.

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REFERENCES

[1] J.-P. Colinge, Silicon-On-Insulator Technology: Materials to VLSI, 3a Edition, Kluwer Academic Publishers, 2004.

[2] J. Shyu, G. C. Temes and K. Yao: Random Errors in MOS Capacitors. IEEE Journal of Solid-State Circuits, v. sc-17, n. 6, p. 1070-1076, 1982.

[3] J. B. Shyu, G. C. Temes, and F. Krummenacher: Random Errors Effects in Matched MOS Capacitor and Current Sources. IEEE Journal Solid-State Circuits, v. sc-17, p. 948-955, 1984.

[4] A. V. Bosch; M. Steyaert and W. Sansen. A High-Density, Matched Hexagonal Transistor Structure in Standard CMOS Tech. for High Speed Applications, IEEE Trans. On Semiconductor Manufacturing, v. 13, n. 2, p. 167-172, 2000.

[5] X. Wang; S. Roy; A. R. Brown and A. Asenov. Impact of STI on Statistical Variability and Reliability of Decananometer MOSFETs. IEEE Electron Device Letters, v. 32, n. 4, p. 479-481, 2011.

[6] Y. Joly; L. Lopez; L. Thruphemu; J-M. Portal; H. Aziza; F. Julien; P. Fornara; P. Masson; J-L. Ogier and Y. Bert. Gate Voltage Matching Investigation for Low-Power Analog Applications. IEEE Transaction On Electron Devices, v. 60, n. 3, p. 1263-1267, 2013.

[7] A. B. Sachid; Y.-M. Huang; Y.-J. Chen; C.-C. Chen; D. D. Lu; M.-C. Chen; C. Hu. FinFET With Encased Air-Gap Spacers for High-Performance and Low-Energy Circuits, vol. 38, n. 1, p. 16 - 19, 2017.

[8] M. C. Robbins; S. J. Koester. Black Phosphorus p- and n-MOSFETs With Electrostatically Doped Contacts, vol. 38, n. 2, p. 285-288, 2017.

[9] S. P. Gimenez. Diamond MOSFET: An innovative layout to improve performance of ICs. Solid-State Electronics, v. 54, issue 1, p. 1690-1699, 2010.

[10] S.P. Gimenez. Invited paper: Innovative Layout Styles to Boost the Mosfet Electrical Performance. In: China Semiconductor Technology International Conference 2014 (CSTIC 2014), 2014, Shangai, China.

[11] S. P. Gimenez; E. D. Neto; V. V. Peruzzi; C. Renaux; D. Flandre. A compact Diamond MOSFET model accounting for the PAMDLE applicable down the 150 nm node. Electronics Letters, vol. 50, p. 1618-1620, 2014.Moore, D. S. The Basic Practice of Statistics, Freeman and Company, 18 ed., New York, 1998.

[12] D. Elias; T. Reshef; O. S. Birk; R. Zee; M. D. Walker; I. R. Cohen. Vaccination against autoimmune mouse diabetes with a T-cell epitope of the human 65-kDa heat shock protein. Proc. Natl. Acad. Sei. USA. Vol. 88, pp. 3088-3()1)1, April 1991. Medical Sciences.

[13] F. Y. Chun; H. Y. Chun; M. X. Min. The application of Student's t-test in internal quality control of clinical laboratory. Frontiers in Laboratory Medicine 1 (2017) 125–128.

[14] R. Guerreiro; D. O. Soutes. Time-based Management Practices: A Study of Brazilian Companies. R. Cont. Fin. – USP, São Paulo, v. 24, n. 63, p. 181-194, set./out./nov./dez. 2013.

[15] R. Larson; B. Farber. Estatística Aplicada, Pearson Prentice Hall, 4 ed, São Paulo, 2010.

[16] M. N. Magalhães; A.C.P. Lima. Noções de Probabilidade e Estatística, EDUSP (Editora da Universidade de São Paulo), 6 ed., São Paulo, 2005.