Numerical Simulation and Analysis of Transistor Channel Length and Doping Mismatching in GC SOI nMOSFETs Analog Figures of Merit

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***Abstract*— This paper presents a two-dimensional numerical simulation study of mismatching on the analog characteristics of fully-depleted graded-channel (GC) SOI MOSFET. The study aims at identifying the mismatching sources that affect the analog performance of GC SOI transistors. The simulations were performed imposing length and doping concentration variations and analyzing its impact on important electrical parameters such as threshold voltage and subthreshold slope, as well as analog parameters, namely transconductance, output conductance, Early voltage and intrinsic voltage gain.**

Keywords—graded-channel transistor; SOI MOSFET; mismatching; numerical simulations.

I. INTRODUCTION

Graded-Channel SOI MOSFET (GC) has been proposed and demonstrated to improve analog characteristics of FD SOI transistors. This device presents asymmetric doping concentration along the channel [1], which is divided in two regions. The first region is highly doped (HD) near the source region and is responsible for fixing the threshold voltage (V_{TH}) of the device. The remaining channel is lightly doped (LD) and acts electrically as an extension of the drain region, as it features lower V_{TH}, reducing the effective channel length to practically the length of the highly doped region only (L_{eff}=L-L_{LD}, being L the channel mask length and L_{LD} the lightly doped channel length) while the device is in saturation. A schematic figure of a GC SOI nMOSFET is presented in Figure 1.

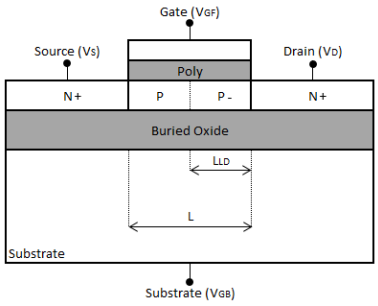

Fig. 1. Schematic cross-section of a Graded-Channel SOI nMOSFET.

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Some advantages of GC SOI devices in comparison to uniformly doped devices at device level are: an increase of drain current (I_{DS}), transconductance (g_m), Early voltage (V_{EA}) and decrease of drain output conductance (g_D) [2, 3]. Taking benefit of these advantages several analog circuits have been successfully fabricated and demonstrated using uniformly-doped and GC SOI devices such as current mirrors [4], source-follower buffers [5] and operational amplifiers [6], with remarkable improvements due to the use of GC SOI.

The concept of matched transistors is one of the most important features in analog circuit design, as several circuits operation rely on the similarity of electrical behavior of close devices. Some few works report information on the matching properties of GC SOI transistors [7, 8, 9]. In [9] present results of experimental mismatching measurements performed using dedicated structures designed with this purpose. All these reported works indicate that, apart from random doping fluctuation and channel length definition, mismatching of GC SOI transistors are also affected by the accuracy of L_{HD}, due to the diffusion of dopant impurities from HD to LD region. However, in experimental data, all these effects occur at the same time and it is difficult to isolate their influence over the electrical parameters. Therefore, in this work numerical simulations are used to evaluate the mismatching of GC SOI MOSFETs , by imposing doping and L_{LD} length variation. The study focus its attention to analog parameters, such as transconductance in saturation, output conductance, intrinsic voltage gain and Early voltage.

II. SIMULATED DEVICE CHARACTERISTICS

The simulated devices present the same characteristics as in [10], using a FD SOI technology with buried oxide thickness (t_{oxb}) of 390 nm, thick oxide gate (t_{oxb}) 30 nm and silicon layer final thickness (t_{Si}) of 80 nm. The lightly and highly doped regions feature doping concentration of N_{AL}=1x10^{15} cm^{-3} and N_{AH}= 5×10^{16} cm^{-3}, respectively. Devices with channel width (W) of 1 µm and total channel length (L) of 2 µm with different L_{LD}/L ratios of 0.2, 0.3, 0.4 and 0.5 were simulated.

Two dimensional numerical simulations were performed through Sentaurus Devices software from Synopsys [11], and were divided into two groups:

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1) The first group kept N_{AH} constant, imposing a variation in HD length (ΔL_{HD}) of ±30nm for each L_{LD}/L ratio. This variation has been chosen following the conclusions of [7] The percentage of L_{LD}/L variation were between 1.875% and 3%, depending on the device, as can be seen on Table I.

TABLE I. PERCENTUAL VARIATION OF ±30NM IN L_{HD}.

L_{LD}/L	L_{HD} [µm]	$\sigma L_{HD}/L_{HD}$ [%]
0.2	1.57-1.63	1.875
0.3	1.37-1.43	2.143
0.4	1.17-1.23	2.500
0.5	0.97-1.03	3.000

2) The second group kept total length and the L_{LD}/L ratio fixed and a variation in HD doping concentration (ΔN_{AH}) of ±10% for each device.

As the source of process variation that may cause total channel length mismatching is the same between uniformly-doped and graded-channel transistors, this parameter has not been changed in this work.

III. NUMERICAL SIMULATION RESULTS AND DISCUSSION

From simulated I_{DS} *versus* V_{GF} curves biased at V_{DS}=50 mV with 1mV step, the subthreshold slope (SS) values were extracted and its standard deviation was calculated as can be seen on Table II.

As the L_{LD}/L ratio increases one can notice a slightly degradation of the subthreshold slope, both when doping of L_{LD} length were varied. For both variations the mean value of the subthreshold slope has not been significantly affected but a higher variation of its value is seen when N_{AH} was varied in comparison the SS standard variation L_{HD} variation was imposed. This indicates that subthreshold slope variation among identically designed devices are originated mainly from variations of doping concentration and in GC devices, is not affect by any imprecision on the L_{HD} definition.

TABLE II. SUBTHRESHOLD SLOPE AND SUBTHRESHOLD SLOPE STANDARD DEVIATION EXTRACTED FROM THE MEAN CURRENT CURVES.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	S_{mean} [mV/dec]	$\sigma S/S_{mean}$ [%]	S_{mean} [mV/dec]	$\sigma S/S_{mean}$ [%]
0.2	65.7	0	65.7	0.30
0.3	66.2	0	66.1	0.31
0.4	67.2	0	66.9	0.48
0.5	68.3	0	68.3	0.44

The same trends were obtained for the threshold voltage, extracted using the double derivative of I_{DS} *versus* V_{GF} with V_{DS}=50 mV, which are presented in Table III.

TABLE III. THERSHOLD VOLTAGE AND THERSHOLD VOLTAGE STANDARD DEVIATION EXTRACTED FROM THE MEAN CURRENT CURVES.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	V_{thmean} [mV]	$\sigma V_{th}/V_{thmean}$ [%]	V_{thmean} [mV]	$\sigma V_{th}/V_{thmean}$ [%]
0.2	319	0.18	319	18.35
0.3	316	0.18	316	18.53
0.4	311	0.32	311	18.97
0.5	304	0.33	304	19.26

As the L_{LD}/L ratio increases the mean threshold decreases, due to the reduction of effective channel length. However, V_{TH} mean value is not affected by ΔN_{AH} or ΔL_{HD}. Looking at the standard variation, one can see that the percentage of V_{TH} variation is lower than the imposed ΔL_{HD} variation (maximum value is 3%, as shown in Table I). On the other hand, by applying a variation of 10% in ΔN_{AH}, V_{TH} variation in larger than 18%. This indicates that the threshold voltage standard variation is originated mainly from variations of doping concentration and that the effective length variation does not play a significant role.

Figure 2 presents the drain current relative deviation as a function of the gate overdrive ($V_{GT}=V_{GF}-V_{TH}$) for ΔL_{HD} (top) and ΔN_{AH} (bottom) variation, with V_{DS}=50mV. As can be noticed, as in any MOSFET, the standard variation is higher when the device operates in weak inversion due to the V_{TH} mismatch influence at low V_{GT}. As the V_{GT} increases the V_{TH} mismatch becomes less important and the current mismatching tends to a constant value. In strong inversion the standard deviation is basically the same for every L_{LD}/L ratio, for both variation applied. At V_{GT}=3V the standard deviation is smaller than 0.4% for ΔL_{HD} and 2% when ΔN_{AH}. When in weak inversion the standard variation becomes dependent on L_{LD}/L ratio when L_{HD} is varied (reaching up to 10% at V_{GT}=0 with L_{LD}/L=0.5) but when the variation is imposed to N_{AH} no dependence with L_{LD}/L is observed, although the relative deviation has an important degradation, reaching 140%.

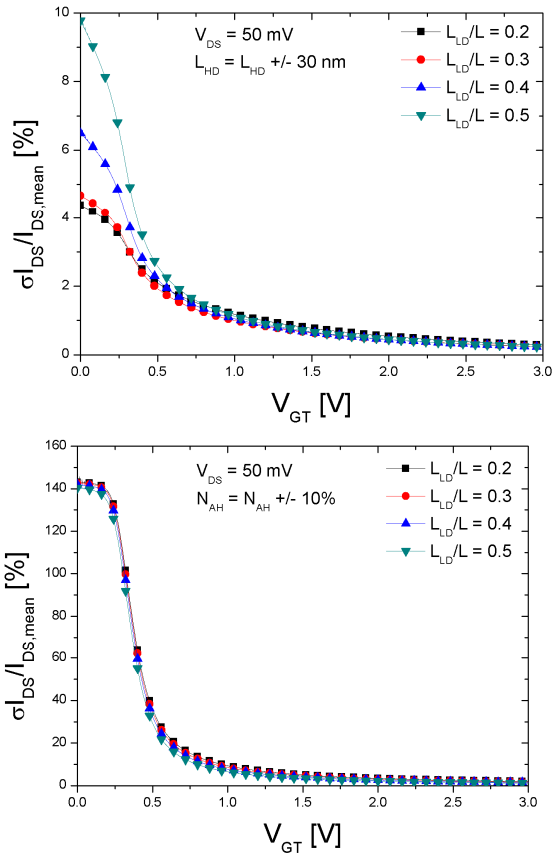

Fig. 2. *Relative standard deviation of drain current as a function of the gate voltage overdrive measued at V_{DS}=50 mV for ΔL_{HDeff} (top) and ΔN_{AHeff} (bottom).*

Figure 3 presents the transconductance relative deviation as a function of the gate voltage overdrive for devices biased at V_{DS}=1.5V, for ΔL_{HD} (top) and ΔN_{AH} (bottom) variations. As the V_{GT} increases the standard deviation decreases and tends to be constant at values lower than 1%, for both variations applied. Table IV presents the transconductance mean values and relative deviation at V_{GT}=200mV and V_{DS}=1,5V. One can notice that the mean values increases as the L_{LD}/L ratio increases as reported in the literature, and the mean values are about the same, independent on the variation that has been imposed. When the results ΔL_{HD} is observed, one can see that the standard variation increases as L_{LD}/L ratio increases, but for ΔN_{AH} this tendency is opposite. The standard deviation for ΔL_{HD} are basically the same as the variation imposed, whereas for ΔN_{AH} the standard variation is lower than variation imposed. This indicates that in experimental devices, the transconductance standard variation must be a combination of these two effects, with the variation of channel length being more pronounced as the effective channel length is reduced (L_{LD}/L increase).

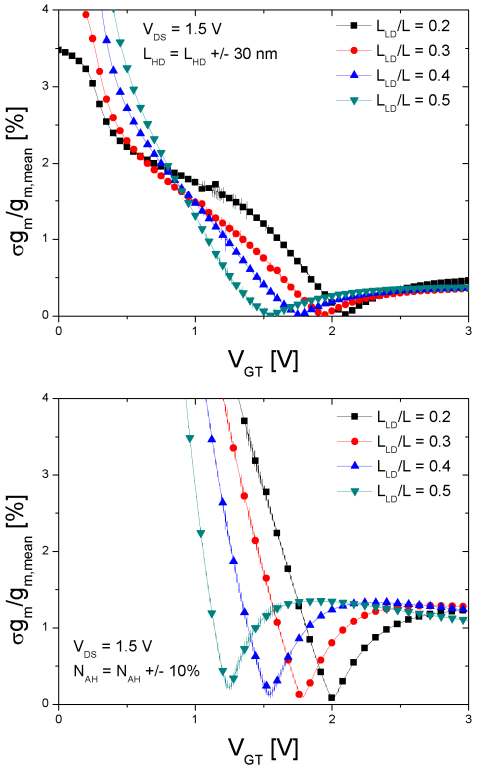

Fig. 3. *Relative standard deviation of transconductance as a function of the gate voltage overdrive measued at V_{DS}=1.5 V for ΔL_{HDeff} (top) and ΔN_{AHeff} (bottom).*

TABLE IV. MEASURED MEAN TRANSCONDUCTANCE AND TRANSCONDUCTANCE STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L	ΔL_{HDeff}		ΔN_{AHeff}	
	$g_{m,mean}$ [µS]	$\sigma g_m/g_{m,mean}$ [%]	$g_{m,mean}$ [µS]	$\sigma g_m/g_{m,mean}$ [%]
0.2	7.5	1.96	7.59	1.82
0.3	8.71	2.02	8.68	1.44
0.4	10.28	2.26	10.23	0.86
0.5	12.60	3.21	12.68	0.48

Figure 4 presents the relative deviation of the drain current as a function of V_{DS}, for devices biased at V_{GT}=200mV when ΔL_{HD} (top) and ΔN_{AH} (bottom) variations are promoted. The presented results show that the standard deviation stays practically constant when in saturation, for both variations applied. The drain current standard deviation is slightly larger when L_{HD} in varied, in comparison the results of N_{AH} variation.

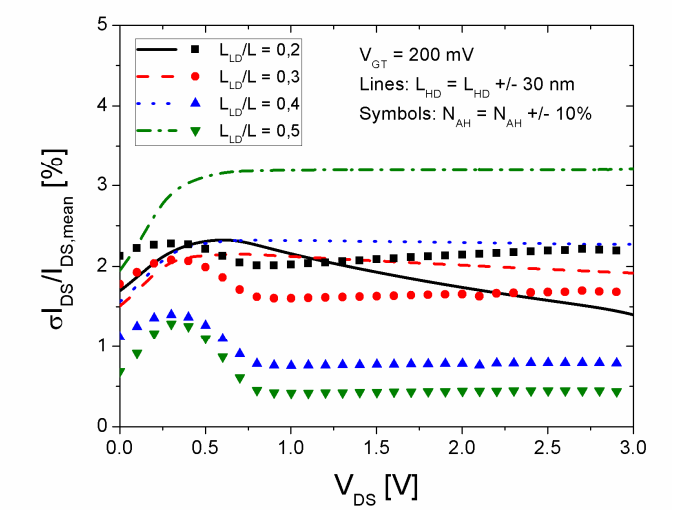

Fig. 4. *Relative standard deviation of drain current as a function of the drain voltage measued at V_{GT}=200 mV for ΔL_{HDeff} (top) and ΔN_{AHeff} (bottom).*

From each drain current curve as a function of drain bias, the output conductance (g_D) has been extracted at V_{GT}=200mV and V_{DS}=1.5V and the mean values and its standard deviation were calculated. The obtained results are presented on Table V. One can notice that the mean values decrease as the L_{LD}/L ratio increases and they are virtually the same independent on the imposed variation (ΔL_{HD} or ΔN_{AH}). The relative standard deviation for ΔL_{HD} decreases as L_{LD}/L ratio increases and its values are higher than the variation imposed (see Table I). Although the g_D relative standard deviation is smaller when ΔN_{AH} is imposed, it increases as L_{LD}/L ratio increases. Also, this variation is lower than the 10% ΔN_{AD} imposed. This indicates that these two sources of mismatching affect the output conductance standard variation and either one can be dominant, depending on the L_{LD}/L ratio.

TABLE V. MEASURED MEAN CONDUCTANCE AND CONDUCTANCE STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L	ΔL_{HDeff}		ΔN_{AHeff}	
	$g_{D,mean}$ [S]	$\sigma g_D/g_{D,mean}$ [%]	$g_{D,mean}$ [S]	$\sigma g_D/g_{D,mean}$ [%]
0.2	21.04	15.65	21.02	7.40
0.3	8.17	11.58	8.37	8.14
0.4	4.09	5.62	4.13	8.30
0.5	4.17	5.11	4.29	9.62

Figure 5 presents the mean Early voltage (V_{EA}=I_{DS}/g_D), one can notice that for both variation the mean values are basically the same. The Early voltage mean values and relative deviation extracted at V_{GT}=200mV and V_{DS}=1,5V are presented in Table VI. As expected, the mean values of V_{EA} increases as the L_{LD}/L ratio increases. Following the trends of g_D, the standard deviation for ΔL_{HD} decreases as L_{LD}/L ratio increases, while

ΔN_{AH} causes the standard deviation to rise as L_{LD}/L ratio increases. For ΔL_{HD} the variation imposed is lower than the standard variation obtained (except for L_{LD}/L of 0.5), for ΔN_{AH} the variation imposed is higher than the standard variation obtained.

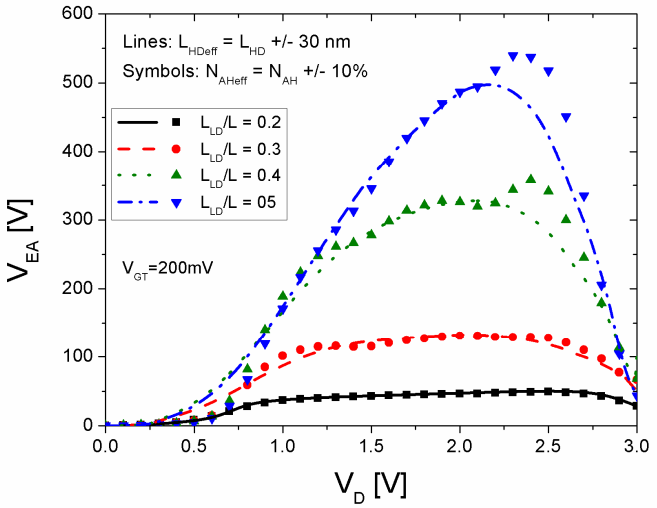

Fig. 5. *Early voltage as a function of the drain voltage measued at V_{GT}=200 mV for ΔL_{HDeff} and ΔN_{AHeff}.*

TABLE VI. MEASURED MEAN EARLY VOLTAGE AND EARLY VOLTAGE STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L	ΔL_{HDeff}		ΔN_{AHeff}	
	$V_{EA,mean}$ [V]	$\sigma V_{EA}/V_{EA,mean}$ [%]	$V_{EA,mean}$ [V]	$\sigma V_{EA}/V_{EA,mean}$ [%]
0.2	43.37	17.61	42.8	5.34
0.3	127.69	14.09	121.3	6.92
0.4	301.15	7.96	289.5	7.76
0.5	367.14	2.05	355.7	9.05

Table VII presents the intrinsic voltage gain ($A_V=g_m/g_D$) mean values and relative deviation at V_{GT}=200mV and V_{DS}=1,5V. One can notice that the mean values increases as the L_{LD}/L ratio increases, which is in accordance to the results reported in the literature. According to Tables, IV and V, the relative variation of g_m and g_D present opposite tendencies. The standard variation of A_V follows the trends shown by g_D, since the decrease of g_D mean value is more pronounced than the increase of mean g_m.

TABLE VII. MEASURED MEAN GAIN AND GAIN STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L	ΔL_{HDeff}		ΔN_{AHeff}	
	$A_{V,mean}$ [V/V]	$\sigma A_V/A_{V,mean}$ [%]	$A_{V,mean}$ [V/V]	$\sigma A_V/A_{V,mean}$ [%]
0.2	367.23	17.68	362.3	5.58
0.3	1078.46	14.05	1041.9	6.68
0.4	2525.40	7.92	2487.4	7.38
0.5	3022.65	2.42	2973.6	9.09

IV. CONCLUSIONS

This paper presented an evaluation of the sources of mismatching in GC SOI transistors by means of numerical simulations. Focus has been given to the effect of these variation over analog parameters of these devices. Results show that the variation on the channel length and channel doping concentration can influence the relative deviation of several parameters in different trends. ΔN_{AH} has shown to have higher influence on the standard variation of threshold voltage and subthreshold slope, while ΔL_{HD} has higher influence on g_m. Both variations have influence over g_D, V_{EA} and A_V, acting in opposite directions, and depending on the effective channel length, anyone can be dominant. Therefore, it may be possible to reduce the effect of mismatching over the analog parameters of GC SOI transistors for a given technology, by choosing an appropriate L_{LD}/L where both variations compensate each other.

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