Asymmetric Self-Cascode Current-Voltage Constructing Algorithm for Analog Figures-of-Merit Extraction

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***Abstract*—This paper proposes an analysis of a self-cascode I-V constructing algorithm for the extraction of DC analog figures of merit, namely the transconductance, output conductance and intrinsic voltage gain. The algorithm was applied on input tables of measured single Fully-depleted Silicon on Insulator (FDSOI) nMOSFETs and was validated on the measured self-cascode association of these devices. The results show an appropriate accuracy, that reflect trends and values with low error.**

Keywords—FDSOI, Algorithm, Self-Cascode, Asymmetric Self-Cascode.

I. INTRODUCTION

In an amplifying stage of an integrated analog circuit design, with the scaling of devices, parameters such as the output conductance (g_D) and the intrinsic voltage gain (A_V) suffer degradation. One might approach this problem by increasing the channel length of the device, but a longer transistor is not able to provide the same transconductance (g_m) and therefore other Figures of Merit (FoM) like the cutoff frequency will be degraded [1]. Adding several amplifying stages will also compromise the bandwidth.

The self-cascode (SC) is a structure that proposes a good compromise between g_D and g_m, being a usual alternative for analog circuit designers. Its structure is composed of two transistors with short-circuited gate nodes and connected by drain node of one to the source node of the other. This intermediate region operates in floating condition [2]. A scheme of the SC with assigned nodes and nomenclatures is shown in Fig. 1. A node followed by an underscript "D" or "S" indicates the node from the single devices that compose the self-cascode, MD and MS respectively.

The SC implemented in Fully-depleted Silicon-on-Insulator (FDSOI) can benefit from threshold voltage control, as the analog output improves with the increase of the difference between the two threshold voltages of the MS and MD transistors. This type of SC will be referred in this paper as Asymmetric Self-Cascode or A-SC [3], while SC which transistors have similar V_T will be referred to as Symmetric Self-Cascode. In the Asymmetric Self-Cascode, the threshold voltage of the transistor near the drain must be lowered in comparison to the standard V_T.

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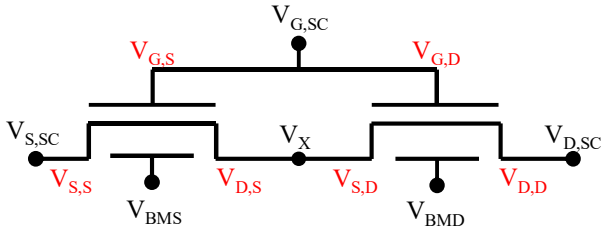

Fig. 1. Self-Cascode Scheme with assigned nodes and nomenclature.

The advantages of this structure have been stated in the literature with comparisons between different technologies, transistor architectures, channel lengths, widths, environment temperatures and applications [3]-[10]. Still, when not fabricated directly on wafer, the characterization of the SC configuration reconstructed by connected single-transistors can be challenging, as it requires space for many probes, may introduce additional errors/parasitics and also require different bias conditions.

In order to circumvent this challenge, allowing the structure test in fabricated single transistors, this paper proposes an approach that allows to reconstruct the self-cascode characteristic curves with accuracy appropriate for further parameter extraction. It uses as input experimental results of single transistors. This approach is here validated with results obtained out of fabricated self-cascodes, implemented in FDSOI technology. Different threshold voltages were obtained by means of different channel doping concentrations on both transistors.

II. SELF-CASCODE STRUCTURE AND PARTICULARITIES

For correctly predicting the behavior of the SC, its working conditions must be established. For simplicity, this section will focus on self-cascodes composed by nMOSFETs and on the nodes of the single transistors.

Looking at the schematic representation of SC presented in Fig. 1, and considering a grounded source node, one can see that the gate voltage of the structure ($V_{G,SC}$) is the same as the gate voltage of MS ($V_{G,S}$). Because of the presence of MD, the drain voltage of the structure will decrease until reaching its

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intermediate node value (V_X), that is the drain node of transistor MS, and is also the source node of transistor MD. A relatively accurate prediction of V_X behavior can be achieved by considering the following constraints, which are natural of the operation of the self-cascode:

- $V_{G,SC} = V_{G,S} = V_{D,S} + V_{G,D}$;
- $V_{D,SC} = V_{D,S} + V_{D,D}$;
- $I_{D,SC} = I_{D,S} = I_{D,D}$.

III. Self-Cascode I-V Constructing Algorithm

The flow of the developed algorithm is described in Fig. 2. First, the tables containing the results obtained through measurements of MD and MS transistors are loaded. Then, a primary search through the input tables is done, looking for matches to the voltage constraints. Then, duplicates of $V_{G,SC}$ or $V_{D,SC}$, depending on the target I-V curve, are eliminated, on the basis of keeping only best fitting on the current constraint. With this, an unrefined I-V curve is obtained.

The refining process is done by interpolation of the input values, to reduce the step of $V_{D,S}$, $V_{D,D}$ and $V_{G,D}$. The range of the input result tables are the ones established by the unrefined output table. With the new refined result tables of MS and MD, the SC table is again constructed by searching though these tables for constraint matches and eliminating worst fitting duplicates.

Using this method, a sufficient accuracy for saturation and above threshold regimes, essential for analog applications, could be achieved. The implementation of this algorithm was done using Matlab [11].

IV. Validation of the Algorithm

The validation of this method was done for FDSOI nMOSFETs fabricated at UCLouvain [12]. The transistors channel lengths are 1 µm and 10 µm. Channel width is 20 µm. The threshold voltages are as shown in Table I. The measured steps of the single devices biases were 10 mV for both V_G and V_D, between -1 V and 2 V range.

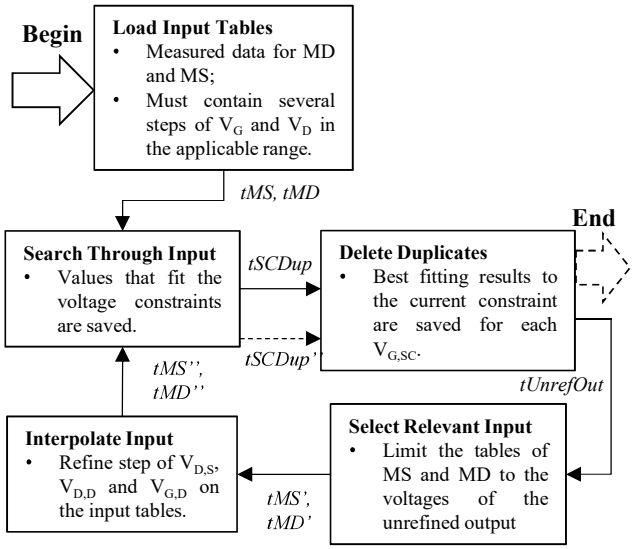

Fig. 2. Schematic of the flow of the algorithm.

TABLE I. Threshold Voltages of Single Devices

Device	Channel Length (µm)	V_T (V)
MS	1.0	-0.1
MD	1.0	-0.75
	10.0	-0.75

A. Characteristic Curves

The I_D as a function of V_G curves for several values of V_D are presented in the Fig. 3. One can see that the overall behavior of the self-cascode current-voltage curve is properly constructed by the algorithm. To further investigate the accuracy of the algorithm, the g_m, extracted from the derivative of I_D as a function of V_G, is presented as a function of V_G on Fig. 4. Although that the results are fitting trends for both self-cascodes, the g_m values are less stable for the longer SC, due to the reduced drain currents. These particularities are more prominent when the SC is operating in a triode regime, which is not within the scope of the analog FoM extraction.

The I_D as a function of V_D curves for several values of V_G are showcased in Fig. 5. The behavior of the drain current is correctly predicted as a function of the drain voltage. The g_D as a function of V_D is presented in Fig. 6 and it shows that there is some instability for the SC composed by longer channel devices. Even so, the order of magnitude of g_D is properly predicted. The verification of the values of g_m and g_D will be more clearly done in the following section.

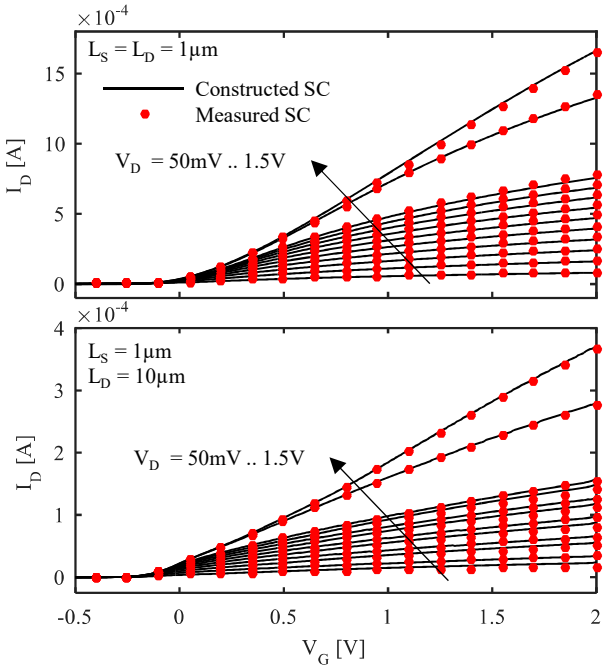

Fig. 3. Drain Current as a function of the gate voltage for self-cascodes composed by MS and MD with different channel lengths and threshold voltages.

B. Analog Figures of Merit

The transconductance as a function of V_D is presented in Fig. 7. It can be seen that the values are predicted with an error of 6% at the worst case for the shorter A-SC. For the longest SC, the highest error at saturation is of 15% and was found for V_G of 0.4 V and V_D of 1 V. In Fig. 8, the g_D is presented as a function of V_G. The accuracy was the best for the higher V_D of 1.5V and the error is the highest for V_G of 0.4 V and V_D of 1V, reaching 1×10^{-5}S difference.

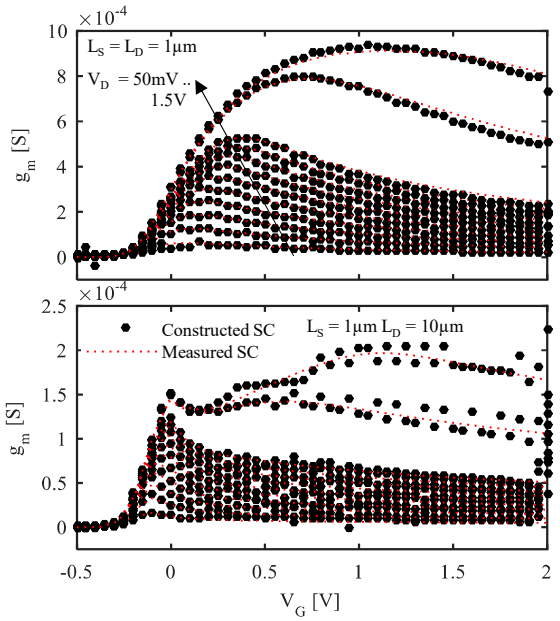

Fig. 4. Transconductance as a function of the gate voltage for self-cascodes composed by MD with different channel lengths.

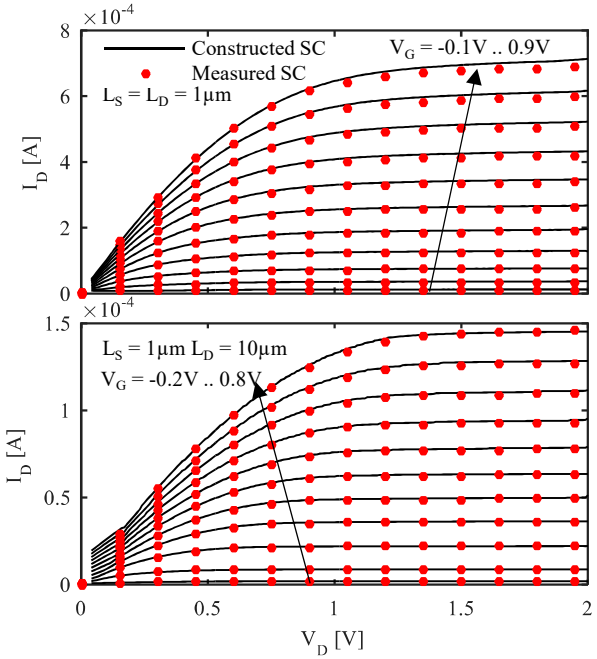

Fig. 5. Drain current as a function of the drain voltage for self-cascodes composed by MD with different channel lengths.

Combining both results, the voltage gain was obtained and is presented as a function of V_G in Fig. 9. Trends and values are accurately predicted.

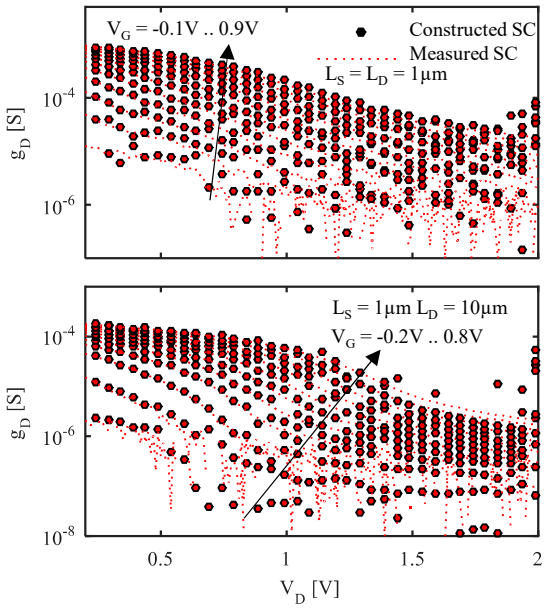

Fig. 6. Output Conductance as a function of the drain voltage for self-cascodes composed by MD with different channel lengths.

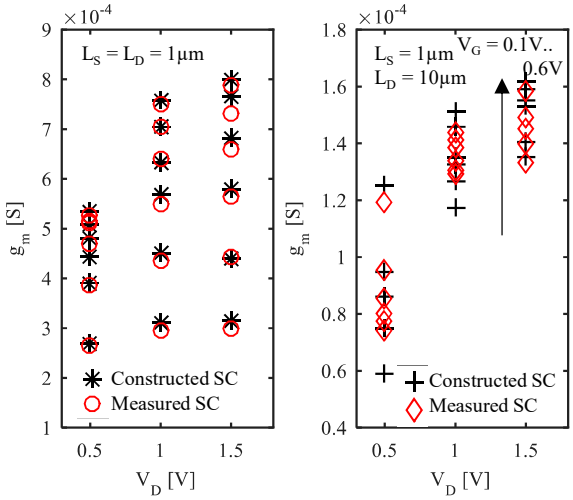

Fig. 7. Transconductance as a function of the drain voltage for self-cascodes composed by MD with different channel lengths.

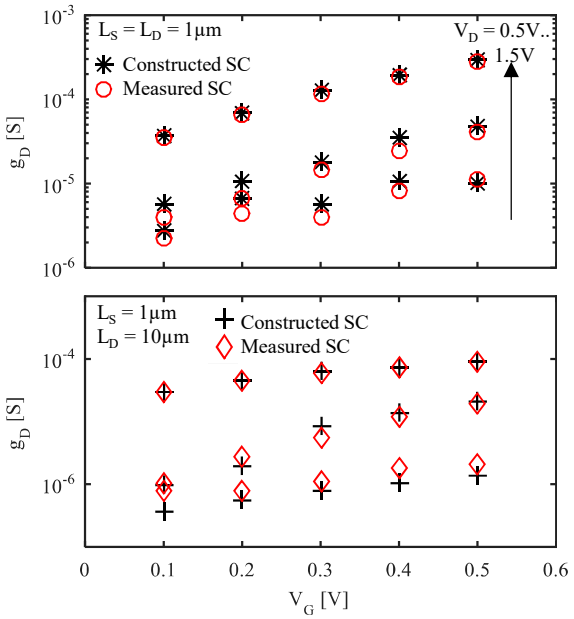

Fig. 8. Output conductance as a function of the gate voltage for self-cascodes composed by MD with different channel lengths.

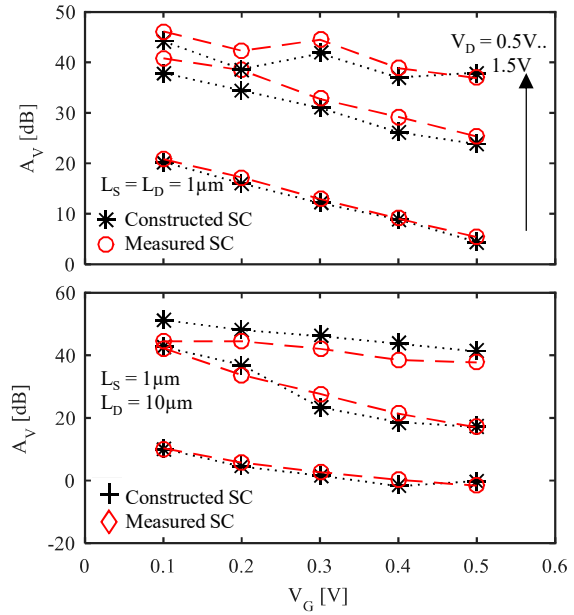

Fig. 9. Voltage gain as a function of the gate voltage for self-cascodes composed by MD with different channel lengths.

V. Conclusion

This paper showcased an algorithmic method to predict the behavior of asymmetric self-cascode structures using the DC I-V characterization of the single devices that compose them. It could be seen that, for saturation regime and for devices operating above threshold, the analog figures of merit g_m, g_D and A_V could be accurately estimated. For the A_V results, the worst case was seen for the longest self-cascode, reaching 6dB error on 44dB of reference value. Thus, this approach can be used for constructing/predicting the SC behavior and DC characterization for these regimes, avoiding a complicated setup in case the fabricated SC is not available.

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