Sizing and Layout Integrated Optimizer for 28nm Analog Circuits Using Digital PnR Tools

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***Abstract*—The design of analog blocks is a bottleneck in a mixed-signal system designs due to the time-consuming layout step needing human intervention at each iteration of the optimization phase. In this paper, we propose a global automatic sizing and layout integrated methodology for analog block sizing including post-layout verification. The proposed optimizer is based on commercial digital place and route tools for the layout step and does not require custom layout procedures or dedicated layout-template framework. An analog cell library in LEF format with transistor, resistance and capacitance layout is used by the PnR tool allowing placement and routing of these elements. A post-layout netlist with parasitic resistances and capacitances as well as proximity effects is then extracted from generated the GDS file for post-layout simulation. A genetic algorithm is implemented as an optimization kernel allowing automatic sizing iteration. The optimizer is demonstrated in an advanced 28nm FDSOI process on typical analog blocks (two-stage basic amplifier, low-noise amplifier, ΔV_T voltage reference and digital-controller oscillator).**

I. Introduction

The increasing complexity of low-power mixed-signal System-on-Chip (SoC) integrating digital and analog blocks presents an growing challenge for the designer. Indeed, although CAD tools for time-efficient design of digital circuits are widely used, analog design is still missing this automation level. In addition to reducing the time-to-market and the development costs, an automated design flow could also allow for an efficient optimization of the Performance-Power-Area (PPA). However with technology scaling, layout effects deteriorate increasingly the performances of analog blocks reducing the design window and forcing post-layout optimization. As shown in Fig. 1 a 50% transition frequency reduction is observed on a basic common-source amplifier stage operated at 1V due to layout effects in 28nm FDSOI. Thus, the optimization loops including layout step must be integrated into the design flow to compensate the loss of performances due to parasitic layout effects. Unfortunately, the absence of mature commercial CADs tools targeting the layout of analog blocks requires time-consuming human interventions and generates a bottleneck in the design flow especially for advanced technologies with a high number of layout design rules. For these reasons, the demand for a layout-aware analog sizing tools is increasing.

Several works have developed specific tools allowing automatic iterations without human intervention [1]-[5]. However, most of these tools are designed for dedicated analog blocks and need layout template frameworks or custom tools limiting their adoption in the industry. In this paper, we propose a global methodology with an automatic sizing-and-layout integrated analog optimizer using commercial digital PnR tools.

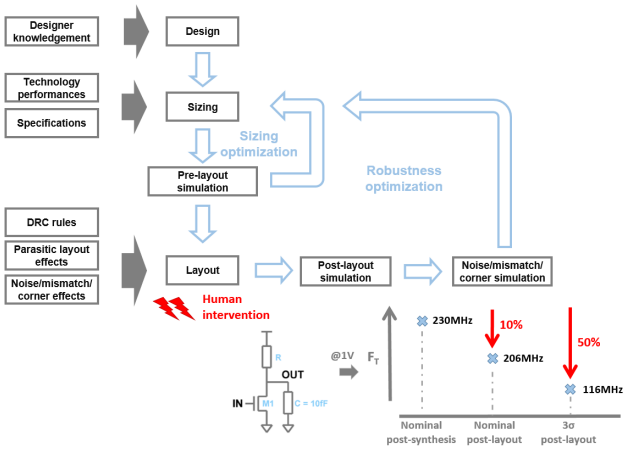


Fig. 1: Conventional design flow including post-synthesis and post-layout iteration along with the transition frequency reduction simulated for a common source at 1V when going to post-layout and Monte-Carlo simulations.

This paper is organized as follows. Section II exposes the integrated optimizer including genetic algorithm kernel, automatic layout generation, parasitic extraction and performance verification. Then, Section III introduces four typical analog blocks that we use as benchmarks for testing the optimizer. Section IV shows the results. We then conclude this paper in Section V.

II. Layout-Aware Analog Optimizer

As shown in Fig. 2, the sizing and layout integrated optimizer is based on a genetic optimization algorithm kernel implemented on Matlab. Non-dominated Sorting Genetic Algorithm II (NSGA-II) [6] is a popular algorithm used in other proposed analog sizing methodologies such as [5]. A random population is combined with the previous-iteration parent population after mutation and cross-overs operation to generate a Pareto curve. Adding a random population differs from the original algorithm but allows to start the optimization without having to ensure that the starting point is feasible. The designer provides the circuit topology, the parameter ranges and the number of iterations which can be modified during the process depending on the evolution of the Pareto

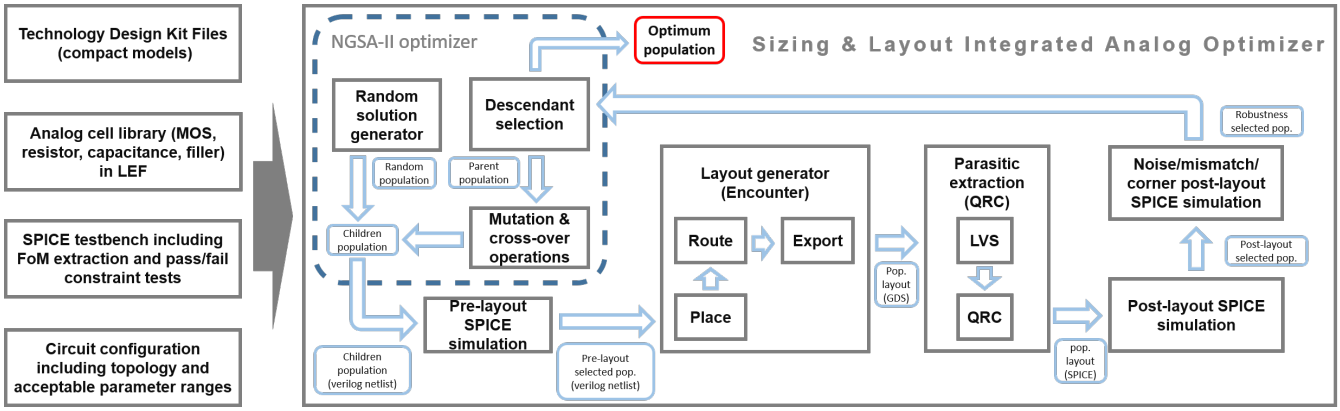


Fig. 2: Proposed sizing and layout integrated optimizer using commercial digital CAD tools.

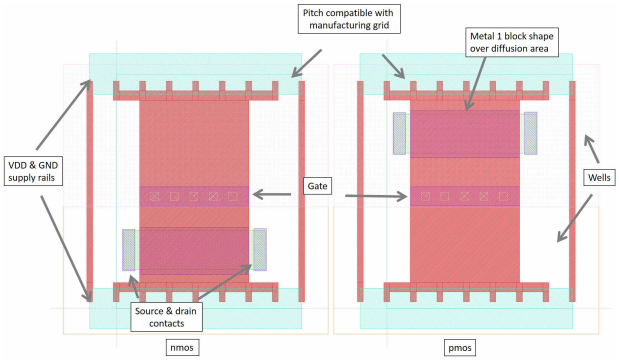


Fig. 3: Example of compatible manufacturing grid pitch thin oxide LVT NMOS and PMOS transistor layout included in the LEF file.

curve. For simulation, a verilog netlist compatible with the SPICE simulator is generated for each new element of the population. When operating on highly-constrained problems, a pre-selection of solutions by a quick functional (DC or AC) simulation is required to avoid the layout step for non-functional solutions and thus speed up the global optimization process.

To generate the layout, the pre-selected population is supplied to the Encounter i.e. the digital PnR tool from Cadence. In order to complete the placement step, we generated a library of analog cells in a LEF layout format for a wide range of sizing parameters and for each sizing possibility and for the 4 basic elements: thick-oxide I/O low-V_T devices, thin-oxide low-V_T (LVT) devices, Metal-Insulator-Metal (MIM) capacitors and poly resistors. As shown in Fig. 3, analog cells contain two power supply rails and respect the manufacturing grid pitch ensuring layout compatibility with a potential digital controller for the analog block. The poly-oxide shape and diffusion area are adjusted in function of the length and the width of the transistor. Moreover, a metal-1 blockage has been added to prevent routing over transistor devices to improve layout matching. The size of the floorplan is automatically adjusted by the PnR tool. For the routing step, the timing analysis is bypassed thanks to a pseudo timing library and the routing optimization is focused on the reduction of routing capacitances. At the end of the place and route step, the GDS file is merged with the basic cell GDS library and exported to the parasitic extraction tool. Then, the parasitic extraction generates a SPICE netlist including parasitic resistances, capacitances and inductances depending on the designer needs. Finally, the post-layout simulation with robustness analysis including mismatch, noise and corners allows to figures of merit defined as the optimization objectives and to test the specification constraints as defined in the testbench.

III. Benchmark

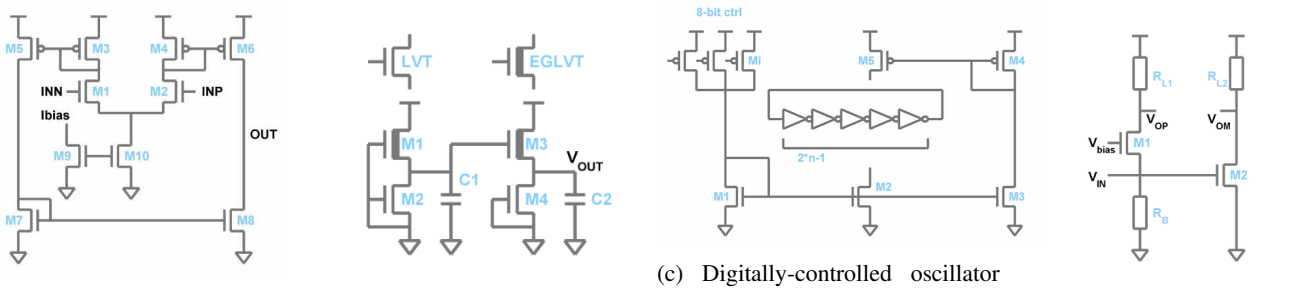
We demonstrate the developed design flow in a 28nm FDSOI technology that has been proven to be a promising candidate for high performance and ultra-low power analog applications for both digital and analog circuits [10]. We chose 4 basic circuits to cover various types of sizing problems appearing when designing analog/RF blocks.

A. Two-stage amplifier

The two-stage amplifier shown in Fig. 4a, is a well-known architecture requiring AC and DC simulations. We assume identical width and length for the differential input stage but we let the choice to the optimizer for the width and the length for other transistors. The design has thus, 11 degrees of freedom for the transistor sizes and for the current bias. The factors of merit are the gain and the transition frequency with constraints on power, slew rate and phase margin.

B. DC Voltage Reference

The DC voltage reference shown in Fig. 4b is a ΔV_T architecture based on V_T difference of two subthreshold-biased transistors. The ΔV_T is implemented with thick- and thin-oxide low-V_T devices based on oxide thickness difference [8]. The external constraint forces specifications imposes a 0.2-0.5V output voltage from a 1V supply. The factors of merit to optimize are the power consumption and the output voltage mismatch which must be both minimized and the degrees of freedom are the size of the four devices.



(a) Two-stage amplifier [7] (b) ΔV_T voltage reference [8] (c) Digitally-controlled oscillator (DCO) (d) Noise-canceling LNA [9]

Fig. 4: Test-circuits benchmark.

TABLE I: Two-stage amplifier specifications

	Sim.	Min. value	Max. Value
DC gain (dB)	AC	40	Max
Phase margin (°)	AC	60	-
f_T (MHz)	AC	10	Max
Slew rate (mV/ns)	DC	10	

TABLE II: DC voltage reference specifications

	Sim.	Min. value	Max. Value
V_{OUT} (V)	DC	0.2	0.5
Power (μW)	DC	Min	-
PSRR @10MHz (dB)	AC	20	-
$\sigma_{V_{OUT}}$ (V)	MC DC	Min	0.1

TABLE III: DCO specifications

	Sim.	Min. value	Max. Value
Power(mW)	Tran.	Min	-
Freq@FF-40°C(MHz)	Tran.	-	200
Freq@SS85°C(MHz)	Tran.	300	-
Transition time (ps)	Tran.	Min	-

TABLE IV: LNA specifications

	Sim.	Min. value	Max. Value
DC gain (dB)	AC	15	-
BW (GHz)	AC	2	-
IIP3 (dbm)	FSST	0	-
NF (dB)	NOISE	Min	-
Power (mW)	DC	Min	-

C. Digitally-controlled oscillator

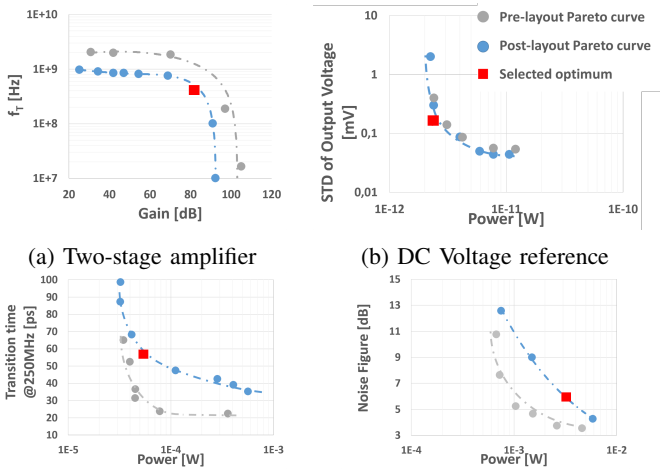
The digitally-controlled oscillator shown in Fig. 4c, is designed to generate a clock with an 8-bit programmable frequency between 200MHz and 300MHz. The circuit is based on a current-starved ring oscillator controlled by an 8-bit current DAC controller. A clock divider followed by a counter allows a regulation by the digital controller during a specific phase. The factors of merit are the power and the edge sharpness which can be linked to the phase noise [12]. The degrees of freedom are the number of stages and the size of the 2 inverter transistors. We assume that the stages are identical.

D. Noise canceling low-noise amplifier

As shown in Fig. 4d, we chose a simple wideband balun-LNA using the noise-canceling topology from [11] and designed in 28nm FDSOI in [9]. This architecture offers low second-order distortion, high supply noise rejection and a compatibility with a following mixer thanks to its differential output [9]. As objectives, we choose to minimize the noise figure and the total power while considering as constraints a 50Ω input matching, 15dB voltage gain and the 3rd order non-linearity (IIP3) over 2dBm. The sizing parameters are the size of both transistors and the value of 3 resistors.

IV. Results

The results presented in this paper, are obtained with a Intel(R) Xeon(R) CPU E5-2630 v3 @ 2.40GHz workstation with 64GB of RAM memory. Ten parallel threads with dedicated CPU are used. At each iteration, NSGA-II testes a population



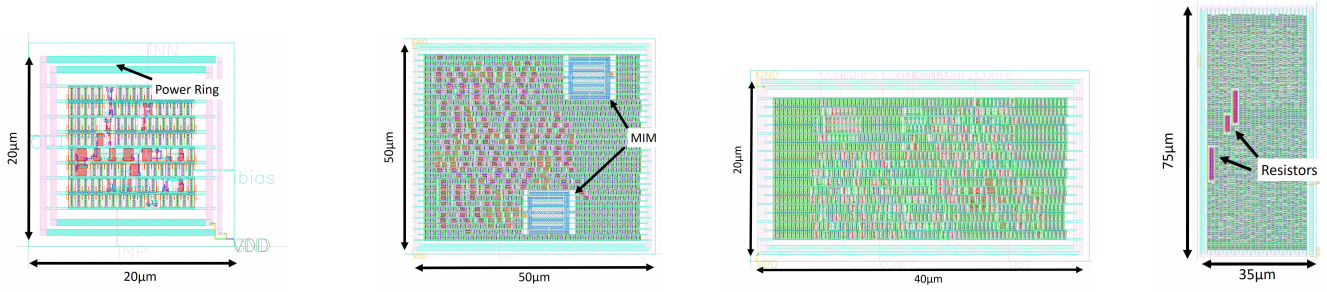
(a) Two-stage amplifier (b) DC Voltage reference

(c) Digitally-controlled oscillator (d) Low-noise amplifier

Fig. 5: Evolution of Pareto curves including layout step in the design flow.

including 50 new solutions built on the parent population with a 0.2 mutation rate and 0.5 cross-over rate. The optimization is completed after 50 iterations.

Fig. 5 shows the Pareto curve for pre-layout and post-layout results and quantifies the loss of performances due to the layout effects confirming the necessity to include the post-layout verification step in the optimization flow. The voltage reference is less sensitive to layout effetcs because wiring capacitances do not affect the DC performances and improve the Power



(a) Two-stage amplifier (b) DC Voltage reference (c) Digitally-controlled oscillator (d) Low-noise amplifier

Fig. 6: Layouts automatically generated by the optimizer.

TABLE V: Final optimum size

Circuit	Final size [μm/μm-Ω-pF-A]	Area overhead
OTA	W1/L1=W2/L2=0.592/0.184 W3/L3=0.648/0.092, W4/L4=0.308/0.044 W5/L5=0.780/0.520, W6/L6=0.296/0.732 W7/L7=0.612/0.780, W8/L8=0.520/0.484 W9/L9=0.908/0.30, W10/L10=0.392/0.300 Ibias=2e-6	x66
DC Ref.	W1/L1=9.7/1, W2/L2=5/1, W3/L3=40.3/1 W4/L4=12.6/1, C1 = 0.9, C2 = 0.9	x6.2
DCO	W_N/L_N=0.368/64, W_P/L_P=764/296 Nbr stage=7, W1/L1=0.280/0.984 W2/L2=0.408/0.340, W3/L3=0.808/0.588 W4/L4=0.456/0.628, W5/L5=0.328/0.908	x30
LNA	W1/L1=100/40, W2/L2=100/40 R_{L1}=166, R_{L2}=155, R_B = 35, V_{biais}	x200

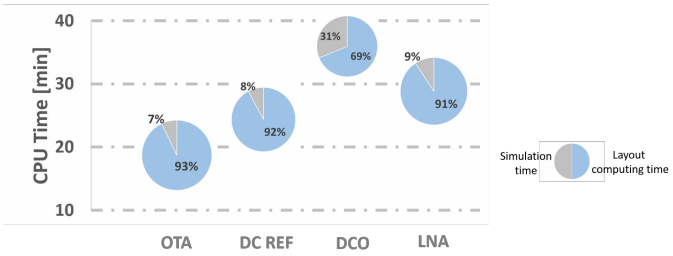


Fig. 7: Average CPU time per iteration.

Supply Rejection Ratio (PSRR). The parameters values for the optimum selected points in Fig. 5, are shown on Table V. As shown in Fig. 6, the placement ignore matching aspect in the design due to the absence of this feature in the classical digital flow but the filler cells increase the uniformity and improve the density allowing improve variability robustness. As mentioned in Table V, the area overhead with an analog floorplan is significant but can be reduced with supplementary efforts during placement step.

As expected, the layout and parasitic extraction steps are both time-consuming processes during an iteration as shown in Fig.7 reaching 92% of the iteration time for AC simulation in the case of the amplifier. In the cases of the DCO optimization requiring two transient simulations and the DC voltage reference requiring Monte-Carlo simulations, we notice that the total computation time is higher than for the cases due to the time-consuming simulations. Computation time required for layout step and parasitic extraction increases with layout size due to the higher number of cells to be placed. We can conclude that the application of this methodology for the sizing optimization of a high level analog block including several low-level blocks, can be improved dividing the sizing problem in several sub-optimizations.

V. Conclusion

We propose an automatic sizing optimizer integrating the layout generation step in the flow based on existing commercial digital CAD tools. Despite an important area overhead and the absence of matching aspect during the placement step, we prove that we can achieve functional analog layouts with descent performances in several hours and in a fully-automated manner.

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