Experimental Evaluation of Mismatching on the Analog Characteristics of GC SOI MOSFETs

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***Abstract*— This paper presents an experimental study of mismatching on the analog characteristics of fully-depleted graded-channel SOI MOSFET in comparison to uniformly doped transistors. The study is carried out using dedicated structures to account for the mismatch that have been fabricated at the same chip and with the same technology. Important basic parameters such as threshold voltage and subthreshold slope were analyzed as well as analog parameters, namely transconductance, output conductance, Early voltage and intrinsic voltage gain.**

Keywords—graded-channel transistor; SOI MOSFET; mismatching; electrical measurements.

I. INTRODUCTION

Graded-Channel SOI MOSFET (GC) is an alternative device for SOI MOS transistors, and presents asymmetric doping concentration along the channel [1], which is divided in two regions. The first region is highly doped (HD) near the source region, and is responsible for fixing the threshold voltage (V_{TH}) of the device. The remaining channel is lightly doped (LD), kept with the natural wafer doping concentration and acts electrically as an extension of the drain region, reducing the effective channel length to practically the length of the highly doped region only (L_{eff}=L-L_{LD}, being L the channel mask length and L_{LD} the lightly doped channel length) while the device is in saturation. A schematic figure of a GC SOI nMOSFET is presented in Figure 1.

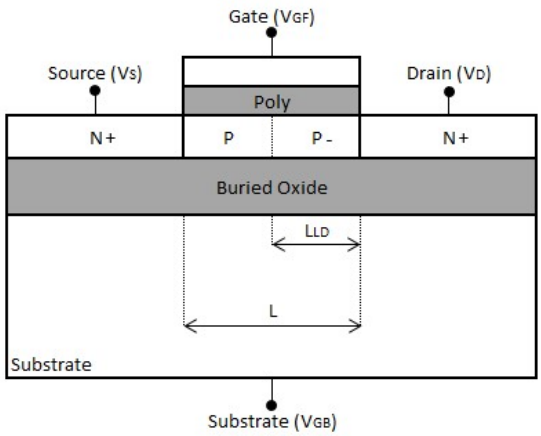

Fig. 1. Schematic cross-section of a Graded-Channel SOI nMOSFET.

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Several papers report advantages of GC SOI devices in comparison to uniformly doped devices, at device and circuit levels. At device level an increase of drain current (I_{DS}), transconductance (g_m), Early voltage (V_{EA}) and decrease of drain output conductance (g_D) have been verified [2, 3]. In addition, some works demonstrated the potential of the graded-channel structures for the application in microwaves [4] and high frequencies [5, 6].

Despite the advantages of Graded-Channel transistors for analog applications, only few works presenting information on the matching properties are available [7, 8]. In this work an experimental evaluation of the mismatching of GC SOI MOSFETs is presented, focusing on analog parameters, such as transconductance in saturation, output conductance, intrinsic voltage gain and Early voltage. Differently of the previous works in [5-6] this study has been carried out with dedicated structures designed for mismatch evaluation minimizing the number of external variations influencing the measured data.

II. TEST STRUCTURE AND DEVICE CHARACTERISTICS

The studied devices were fabricated in a FD SOI technology buried oxide thickness (t_{oxb}) of 390 nm, thick oxide gate (t_{oxb}) 30 nm and silicon layer final thickness (t_{Si}) of 80 nm. The lightly and highly doped regions feature doping concentration (N_{AL}=10^{15} cm^{-3} and N_{AH}= 6×10^{16} cm^{-3}, respectively. Arrays of 20 identically-designed uniformly doped and GC SOI transistors were fabricated. Each device has individual gate, source and drain pads, and present channel width (W) of 20 µm and mask channel length (L) of 2 µm. For Graded-Channel transistors, two different L_{LD}/L ratios were fabricated (L_{LD}/L = 0.25 and 0.375). For uniformly doped devices highly and lightly doped ones, (noted as L_{LD}/L=0 and 1, respectively) have also been fabricated for comparison purposes.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Drain current (I_{DS}) curves were measured as a function of gate (V_{GF}) and drain (V_{DS}) voltages for each transistor. Due to the fabrication process, there might be imprecision on the definition of L_{LD} length. Therefore, the effective L_{LD}/L ratio has been experimentally obtained according to the method described in [1] for each device and the mean effective L_{LD}/L

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and standard deviation are presented in Table I. As can be noted, the standard deviation in the extracted L_{LD}/L increases as the ratio is raised. Initially, I_{DS} *versus* V_{GF} curves were measured at V_{DS}=25 mV with 1 mV-step. The mean drain current curves as a function of gate voltage are presented in Figure 2. As already reported for GC devices, the increase of L_{LD}/L ratio promotes the increase of current level. Besides, there is no degradation of subthreshold slope, as can be noted from the results presented in Table I. The presented values are close to the physical limit of 60 mV/dec at room temperature. These results show that even for the GC device with shorter effective channel length (L_{LD}/L=0.42, that corresponds to L_{eff}=1.16 μm) no important degradation due to short-channel effects has occurred.

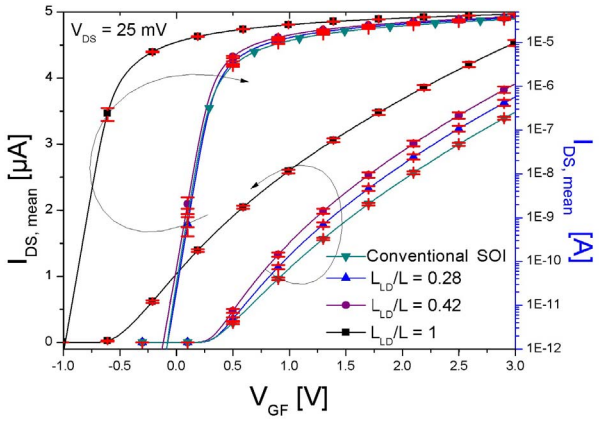

Fig. 2. *Mean I_{DS} versus V_{GF} with V_{DS}=25mV.*

TABLE I. SUBTHRESHOLD SLOPE EXTRACTED FROM THE MEAN CURRENT CURVES.

L_{LD}/L		S_{mean} [mV/dec]
mask	***effective***	
0.000	–	63
0.250	0.264 ± 0.0200	64
0.375	0.393 ± 0.0347	66
1.000	–	68

The threshold voltage (V_{TH}) has been extracted from each measured I_{DS} *versus* V_{GF} curve at low drain bias, using the double derivative method [7]. The obtained mean threshold voltage ($V_{TH,\ mean}$) and its standard deviation (σV_{TH}) are presented for the four different arrays of devices, and the resulting values are presented in Table II.

TABLE II. MEASURED MEAN THRESHOLD VOLTAGE AND THRESHOLD STANDARD DEVIATION.

L_{LD}/L		$V_{TH,\ mean}$ [mV]	σV_{TH} [mV]	$\sigma V_{TH}/V_{TH,\ mean}$ [%]
mask	***effective***			
0.000	–	104.89	6.45	6.15
0.250	0.264 ± 0.0200	127.53	7.93	6.21
0.375	0.393 ± 0.0347	105.26	7.22	6.86
1.000	–	-596.50	12.40	2.08

As can be noted, the threshold voltage values for GC devices are close to that presented by uniformly doped transistors with higher doping concentration in the channel. Also, the relative standard deviation of the threshold voltage ($\sigma V_{TH}/V_{TH,\ mean}$) shows a slight worsening when the graded-channel structure is used, which is related to the channel length reduction as the L_{LD}/L is increased and the larger standard deviation of L_{LD}/L ratio definition, as seen in the results shown in Table I.

According to [9], the relative mismatch in the drain current can be expressed as a function of the mismatch in the threshold voltage and current factor $\left(\beta = \mu_{eff} C_{ox} \frac{W}{L}\right)$, as shown in equation (1), where μ_{eff} is the effective carrier mobility and C_{ox} is the front gate oxide capacitance per unit area.

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{-\Delta V_{TH}}{V_{GF} - V_{TH}} + \frac{\Delta \beta}{\beta} \quad (1)$$

Figure 3 presents the drain current relative deviation ($\sigma I_{DS}/I_{DS,mean}$) as a function of the gate overdrive (V_{GT}), in order to dismiss the different threshold voltage values among the different devices. As expected, the deviation increases when the device operates in weak inversion, due to be more significant the effects of the threshold voltage mismatch at low values of V_{GT} [10]. As the gate voltage increases the threshold mismatching becomes less important in the current level and the deviation tends to a smaller and constant value, related to β. The curves in logarithmic scale allows for observing that even at strong inversion levels, GC devices promotes the worsening of current matching. Since at large values of V_{GT} the predominant component of mismatching is the current factor, one can conclude that there is another source of mismatching in the asymmetric channel device. According to [7] it must be related to the lack of precision in defining the boundary between the two regions with different doping concentrations, as confirmed by the larger of deviation as L_{LD}/L ratio increases.

The relative deviation reduces when devices are biased in strong inversion. For example, at V_{DS}=25mV and V_{GT}=2.5V, the GC SOI transistors with $(L_{LD}/L)_{eff}$=0.42 present $\sigma I_{DS}/I_{DS,mean}$= 1.3% and it slightly decreases when biased in saturation (V_{DS}=1.5V).

Figure 4 presents the transconductance relative deviation $\sigma g_m/g_{m,mean}$) as a function of the gate voltage overdrive for devices biased in saturation. As for the drain current, in weak inversion, the V_{TH} variation causes the worsening of matching. As devices move to strong inversion, the relative deviation reduces and reaches values smaller than the relative deviation of the drain current. Once again, one can see an slightly higher deviation for GC transistors, although all devices have shown $\sigma g_m/g_{m,mean} \leq 1\%$ for $V_{GT} > 1.2V$ approximately.

Table III presents the transconductance mean values ($g_{m,mean}$) and respective standard deviation (σg_m) for all devices biased at V_{GT} = 200 mV and V_{DS} = 1.5 V. These results show that although the standard deviation is worsened in GC devices with same gate L, due to variations in the current factor, the relative deviation ($\sigma g_m/g_{m,mean}$) is only slightly higher in these

devices, since the mean value is increased by the reduction of effective channel length.

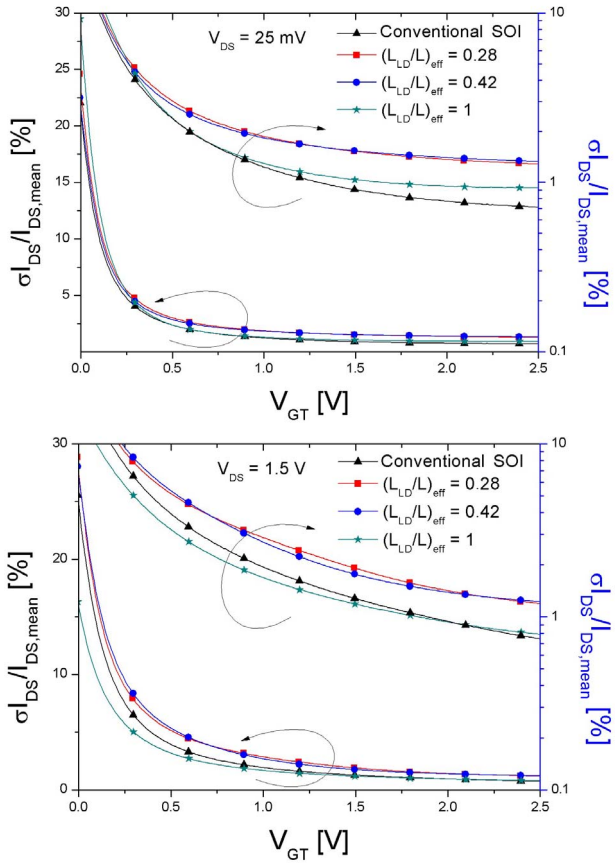

Fig. 3. *Relative standard deviation of drain current as a function of the gate voltage overdrive measued at V_{DS}=25 mV (top) and 1.5V (bottom).*

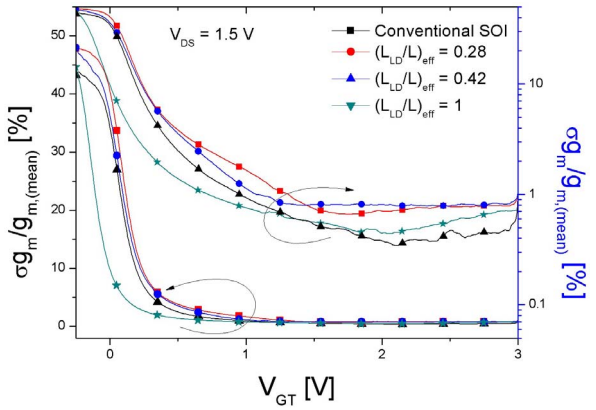

Fig. 4. *Transconductance mismatch as a function of the gate voltage overdrive with V_{DS}=1.5V.*

TABLE III. MEASURED MEAN TRANSCONDUCTANCE AND TRANSCONDUCTANCE STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L		$g_{m,\,mean}$ [µS]	σg_m [µS]	$\sigma g_m/g_{m,\,mean}$ [%]
Mask	*effective*			
0.000	–	141.00	5.98	4.23
0.250	0.264 ± 0.0200	203.00	9.03	4.44
0.375	0.393 ± 0.0347	257.00	12.66	4.91

Figure 5 show the mean current curves as a function of the drain voltage measured at V_{GT}=200 mV. These curves show the increase of current level due to L_{LD}/L ratio increase, apart from the reduction of impact ionization effect, characterized by the additional increase of I_{DS} for V_{DS} larger than 2.5 V in both unfirmly doped devices.

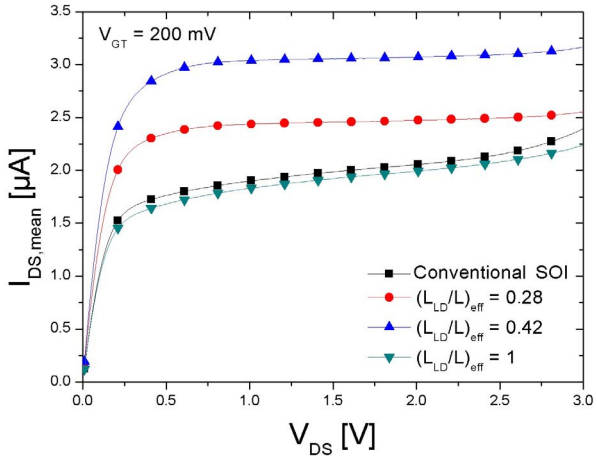

Fig. 5. *Mean I_{DS} versus V_{DS} curves measured with V_{GT}=200mV.*

The relative deviation as a function of V_{DS} is presented in Figure 6 for V_{GT}=200mV and 800mV. The presented results show that the mismatching in saturation is practically constant for the entire applied V_{DS} range. As seen in Figure 3, the L_{LD}/L ratio increases the deviation. Also, the increase of V_{GT} reduces the current mismatching, which is in accordance to the results shown in Figure 3.

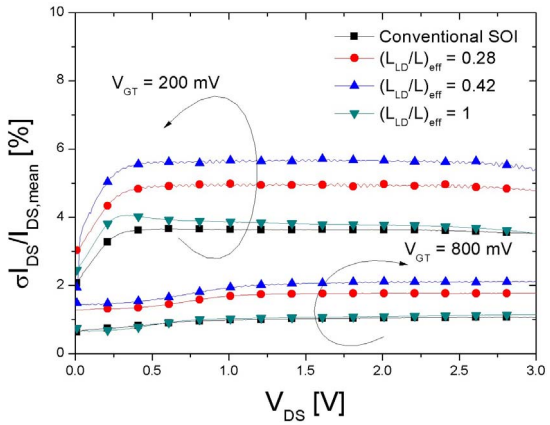

Fig. 6. *Drain current mismatch as a function of the drain voltage with V_{GT}=200mV and V_{GT}=800mV.*

The mean output conductance ($g_{D,mean}$) and its standard deviation (σg_D) extracted at V_{GT}=200 mV and V_{DS} = 1.5 V are presented in Table IV. Contrarily to the results obtained for g_m, the relative standard deviation of g_D ($\sigma g_D/g_{D,mean}$) has shown a significant worsening when the graded-channel structure is used, despite of the smaller σg_D presented by GC devices in comparison to the uniformly doped transistor.

However, when the Early voltage is extracted ($V_{EA}=I_{DS}/g_D$) has been extracted for each device, the resulting relative deviation has shown to be reduced in the entire V_{DS} range. The

mean Early voltage value ($V_{EA,mean}$), as well as it relative deviation are presented in Figures 7 and 8, respectively.

TABLE IV. MEASURED MEAN OUTPUT CONDUCTANCE AND STANDARD DEVIATION FOR DEVICES BIASED AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L		$g_{D,\,mean}$ [S]	σg_D [S]	$\sigma g_D/g_{D,\,mean}$ [%]
mask	*effective*			
0.000	–	1.47×10^{-6}	97.6×10^{-9}	6.63
0.250	0.264 ± 0.0200	0.27×10^{-6}	31.9×10^{-9}	11.6
0.375	0.393 ± 0.0347	0.22×10^{-6}	27.5×10^{-9}	12.4

Although the current and output conductance deviations are worsened in GC devices when compared to uniformly doped ones, the larger value of V_{EA} provided by these devices make the relative deviation become small, and the calculated values have not reached 3% in the whole range of applied V_{DS}.

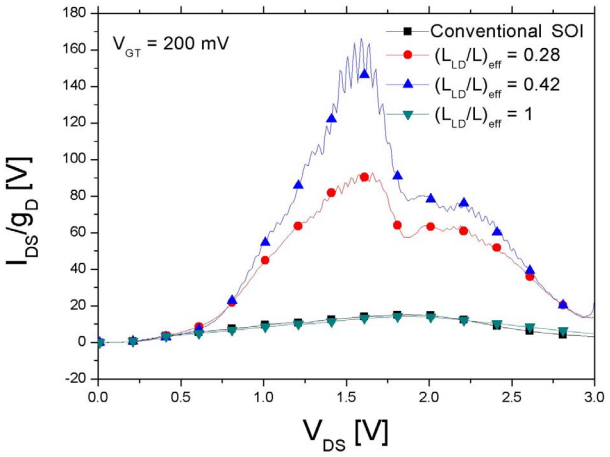

Fig. 7. *Mean Early voltage as a function of the drain current extracted at V_{GT}=200mV.*

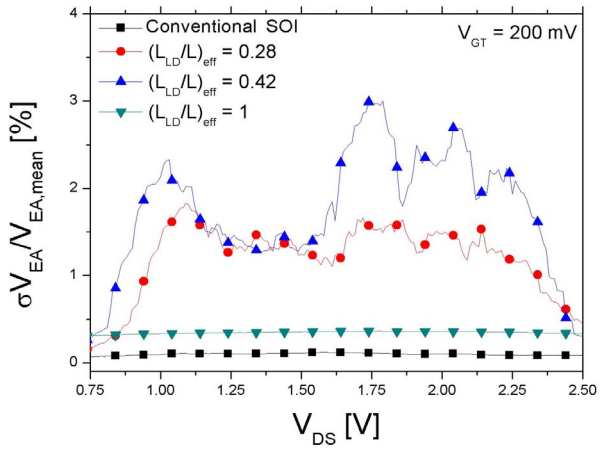

Fig. 8. *Early voltage relative deviation as a function of the drain current with V_{GT}=200mV.*

Finally, the intrinsic voltage gain ($A_V=g_m/g_D$) has been obtained at V_{GT}=200 mV and V_{DS}=1.5 V for each device in order to evaluate the mismatch. The mean value ($A_{V,mean}$) and the standard deviation are presented in Table V. Apart from the increase of $A_{V,mean}$ with the L_{LD}/L rise, one can note the worsening of matching. Although there is an increase in the $\sigma A_V/A_{V,mean}$ with L_{LD}/L rise, the maximum value is in the order of those obtained for $\sigma g_D/g_{D,mean}$ indicating the larger source of mismatch in GC SOI with longer L_{LD} is associated with the mismatch in g_D.

TABLE V. MEASURED MEAN GAIN AND GAIN STANDARD DEVIATION AT V_{GT}=200MV AND V_{DS}=1.5V.

L_{LD}/L		$A_{,\,mean}$ [V/V]	σA [V/V]	$\sigma A/A_{,\,mean}$ [%]
mask	*effective*			
0.000	–	95.99	3.94	4.11
0.250	0.264 ± 0.0200	744.75	73.99	9.93
0.375	0.393 ± 0.0347	1174.63	130.36	11.09

IV. CONCLUSIONS

This paper presents an experimental evaluation of the mismatching effects on analog parameters of GC SOI transistors. Results show that the relative mismatching of GC devices analog characteristics are higher than the conventional transistor. The standard deviation of drain current on GC devices is also slightly higher. The measured mismatch on the output conductance is larger compared to the transconductance mismatch while the device is operating on the region of interest for analog applications. This larger deviation of the output conductance is transferred to the voltage gain leading to similar mismatch in the latter.

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