Channel Width Influence on the Analog Performance of the Asymmetric Self-Cascode FD SOI nMOSFETs

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***Abstract*—In this paper, the analog performance of the Asymmetric Self-Cascode structure of Fully Depleted SOI nMOSFETs has been evaluated with regards to the variation of channel width, through three-dimensional numerical simulations. The largest gain has been obtained using the narrowest transistor near the source and the widest transistor near the drain.**

Keywords—asymmetric self-cascode; channel width; FD SOI nMOSFETs; analog performance; numerical simulations

I. Introduction

The Self-Cascode (SC) configuration, composed by two transistors in series association with short-circuited gates, acting as a single device, is a well-known way of boosting the analog characteristics of MOS transistors [1]. In general, both transistors present the same channel doping concentration. An alternative configuration named Asymmetric Self-Cascode (A-SC) structure, shown in Fig. 1, has recently been proposed, further improving the analog performance of SOI MOSFETs [2, 3]. In this structure, the transistor near the source (M_S) presents larger channel doping concentration, and hence higher threshold voltage (V_{TH}) in comparison with the transistor near the drain (M_D) [2]. In Fig. 1, L_S (W_S) and L_D (W_D) are the channel lengths (widths) of the individual transistors near the source and the drain, respectively. The total channel length (L) of the A-SC structure can be defined as $L_S + L_D$. However since the threshold voltage of M_D is smaller than M_S, the device near the drain has its channel already inverted for gate voltages close to the threshold voltage of the A-SC structure, reducing the effective channel length (L_{eff}) to only L_S [2].

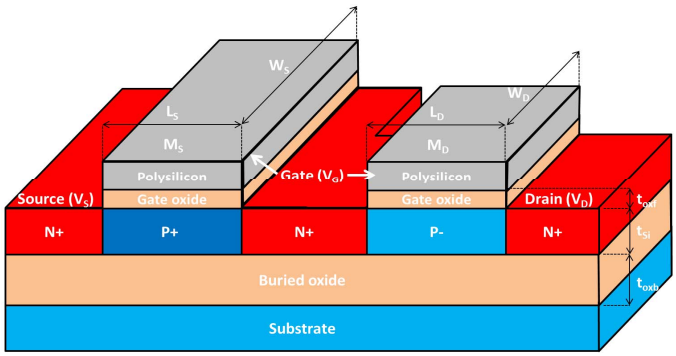

Fig. 1. Asymmetric Self-Cascode structure of FD SOI nMOSFETs.

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The influence of channel length of M_S and M_D transistors has already been addressed at transistor level [3] and in common-source current mirrors [4]. However, no information about the influence of channel width has been reported so far. The goal of this paper is to understand the effects of different W_S and W_D, aiming to obtain the largest intrinsic voltage gain (A_V) and Early voltage (V_{EA}) for the A-SC structure.

II. Devices Characteristics

The measured transistor has been fabricated in a 2µm FD SOI CMOS technology from UCLouvain, Belgium, aiming at the realization of analog read-out circuits co-integrated with MEMS sensors [5]. Each single transistor presents channel length of 2µm and channel width of 20µm. The gate oxide (t_{oxf}), silicon film (t_{Si}) and buried oxide (t_{oxb}) thicknesses are 31, 80 and 390nm, respectively. The M_S transistor presents channel doping concentration of $6\times10^{16}cm^{-3}$, whereas M_D transistor exhibits channel doping concentration of $1\times10^{15}cm^{-3}$.

III. Results

Firstly, the experimental measurements have been used to adjust the simulation parameters. Three-dimensional numerical simulations have been performed with Sentaurus Device software [6]. Fig. 2 presents the drain current (I_D) and the transconductance (g_m) as a function of the gate voltage overdrive ($V_{GT}=V_{GS}-V_{TH}$) for the A-SC (W_S=20µm, W_D=20µm) structure, extracted at V_{DS}=50mV (A) and 1.5V (B). One can notice a good agreement of the simulated I_D and g_m with the experimental curves. The drain current and the output conductance (g_D) are also shown in Fig. 3 against the drain voltage for the same A-SC structure, biased at V_{GT}=200mV. Once again, the simulated results fit the experimental data with good agreement, therefore, validating the analysis of the channel width influence on the analog performance of the A-SC structure through three-dimensional numerical simulations.

Fig. 4 exhibits the drain current and the transconductance as a function of the gate voltage for W_D=1µm varying W_S, extracted at V_{DS}=1.5V. The increase of W_S increments I_D and g_m in the whole gate voltage range, since the transistor near the source dominates the conduction of the A-SC structure, i.e. there is proportionality between the drain current and W_S.

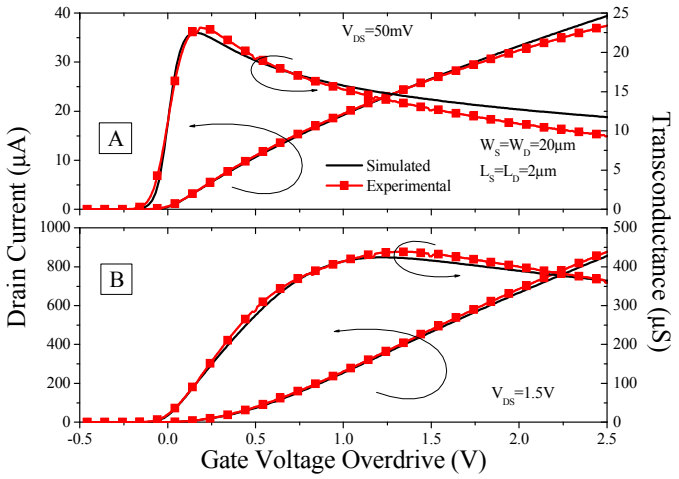

Fig. 2. Drain current (left axis) and transconductance (right axis) as a function of the gate voltage overdrive for the A-SC (W_S=20µm, W_D=20µm) structure, extracted at V_{DS}=50mV (A) and 1.5V (B).

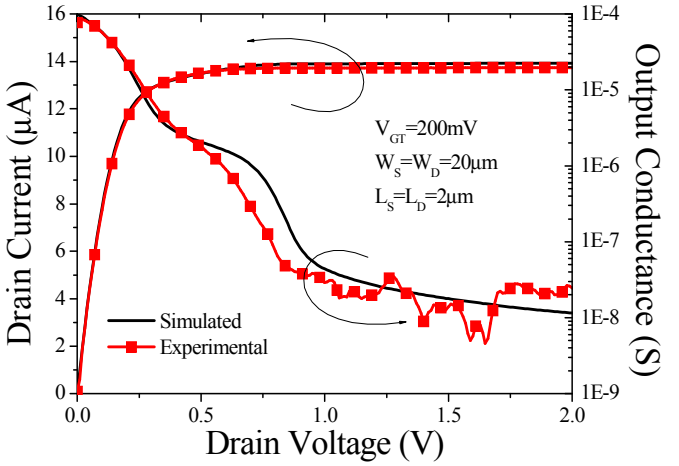

Fig. 3. Drain current (left axis) and output conductance (right axis) as a function of the drain voltage for the A-SC (W_S=20µm, W_D=20µm) structure, extracted at V_{GT}=200mV.

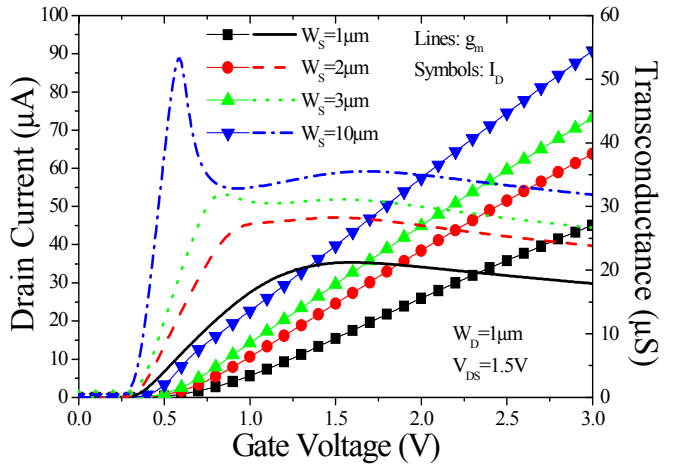

Fig. 4. Simulated drain current (left axis) and transconductance (right axis) as a function of V_{GS} for W_D=1µm varying W_S, extracted at V_{DS}=1.5V.

Fig. 5 analyzes the influence of W_D with fixed W_S=1µm on the transfer characteristics. It is possible to observe at lower V_{GS} that the increase of W_D does not affect I_D and g_m, which is related to the higher electron concentration in the M_D transistor in comparison with the M_S transistor, linked to the lower V_{TH} of the M_D transistor. As stated before, the M_S transistor is the dominant device at low gate voltage. By increasing V_{GS}, M_D starts having influence on I_D, due to the similar electron concentrations in both transistors. In this region, M_D transistor becomes important in the current flow, and as it becomes wider, I_D and also g_m are increased. The wider the M_D, the larger the current level, since its resistance is reduced.

In the case of the A-SC (W_S=10µm, W_D=1µm) structure, one can notice an anomalous behavior of g_m in Fig. 4. In order to understand the presence of two g_m peaks, the intermediate potential between M_S and M_D transistors (V_X) is plotted against V_{GS} in Fig. 6 for W_D=1µm varying W_S, extracted at V_{DS}=1.5V. Analyzing the A-SC (W_S=10µm, W_D=1µm) structure, it is possible to observe a high V_X for V_{GS} close to V_{TH}, which implies in larger I_D and g_m. By increasing V_{GS}, V_X reduces considerably, decrementing g_m. When V_X is stabilized, one can notice an increase of g_m due to the increment of V_{GS} until the moment where the mobility degradation occurs and also the similar electron concentrations between M_S and M_D transistors,

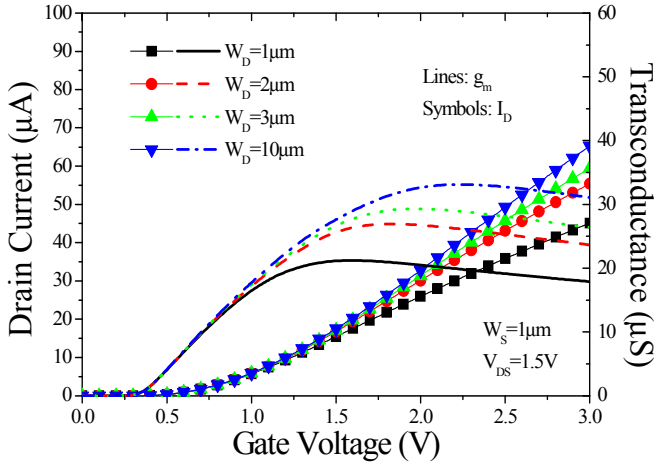

Fig. 5. Simulated drain current (left axis) and transconductance (right axis) as a function of V_{GS} for W_S=1µm varying W_D, extracted at V_{DS}=1.5V.

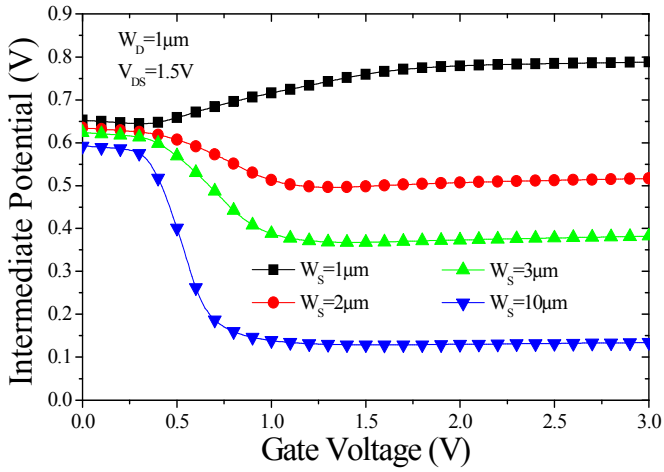

Fig. 6. Simulated intermediate potential as a function of the gate voltage for W_D=1µm varying W_S, extracted at V_{DS}=1.5V.

reducing g_m. In this case, L_{eff} of the A-SC structure is not equal to L_S, but tends to $L_S + L_D$. Besides that, it is possible to see that the intermediate potential saturates for high gate voltage. For the case of the A-SC (W_S=1µm, W_D=1µm) structure, the saturated V_X is approximately equal to half V_{DS}, since the resistances of the M_S and M_D transistors are similar at high V_{GS}, as by the fact of presenting the same aspect ratio (W/L), as of being biased in strong inversion, when the A-SC structure behaves as a uniformly doped transistor with $L = L_S + L_D$. By incrementing W_S, there is a reduction of the resistance of M_S transistor, diminishing V_X. In addition, it is possible to observe that the gate voltage where the saturation of V_X starts goes towards lower V_{GS} as W_S increases in comparison with W_D.

In Fig. 7, the intermediate potential is plotted against V_{GS} for W_S=1µm and several W_D, extracted at V_{DS}=1.5V. By incrementing W_D, the opposite occurs in comparison with Fig. 6, since there is a reduction of the resistance of the M_D transistor, increasing the intermediate potential. Also, one can notice that the gate voltage where the saturation of V_X starts does not change with the increase of W_D.

Fig. 8 presents I_D/W_S as a function of V_{GS} for W_D=1µm varying W_S, extracted at V_{DS}=1.5V. One can verify that I_D/W_S reduces with the increment of W_S. As the dominant device is the M_S transistor at V_{GS} close to V_{TH}, the same normalized drain current would be expected varying W_S. However, in the A-SC structure, both channel widths influence the current flow. By maintaining lower W_D and increasing W_S, there is a larger resistance for the M_D transistor compared with the M_S device, reducing the intermediate potential, as observed in Fig. 6, and hence decreasing the normalized drain current.

Fig. 9 exhibits the drain current and the output conductance as a function of the drain voltage for W_D=1µm varying W_S, extracted at V_{GT}=200mV. As the gate voltage overdrive is reduced, the M_S transistor is the dominant device in the A-SC structure. This way, the increase of W_S increments I_D and g_D.

Based on Fig. 10, where I_D and g_D are plotted against V_{DS} at V_{GT}=200mV for fixed W_S=1µm and several W_D, it is possible to observe that W_D does not influence the drain current level, but reduces the output conductance. This fact can be explained by Fig. 11, where V_X and dV_X/dV_{DS} are presented against V_{DS}

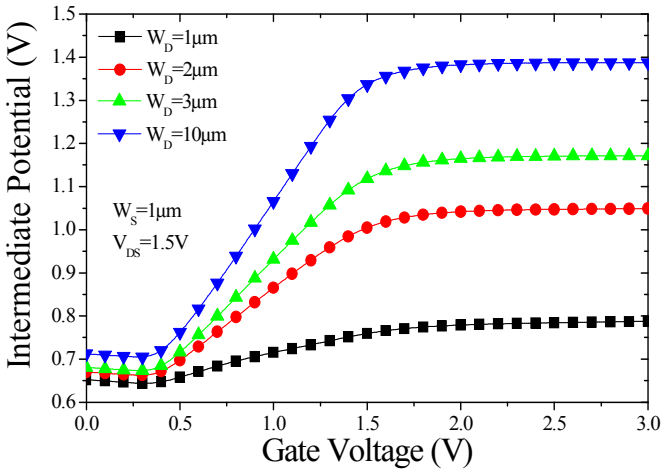

Fig. 7. Simulated intermediate potential as a function of the gate voltage for W_S=1µm varying W_D, extracted at V_{DS}=1.5V.

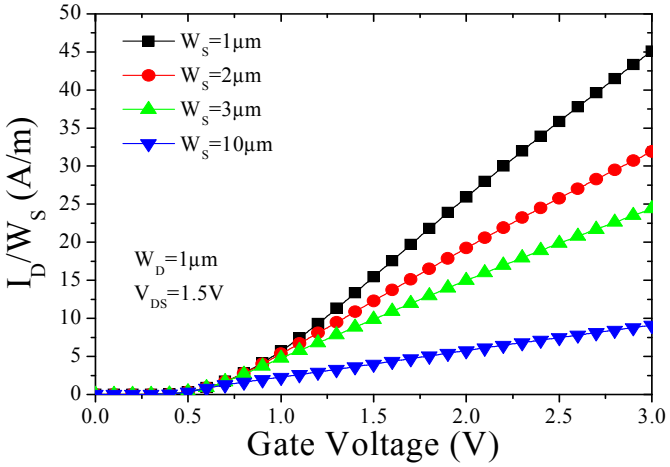

Fig. 8. Simulated drain current normalized by W_S as a function of the gate voltage for W_D=1µm varying W_S, extracted at V_{DS}=1.5V.

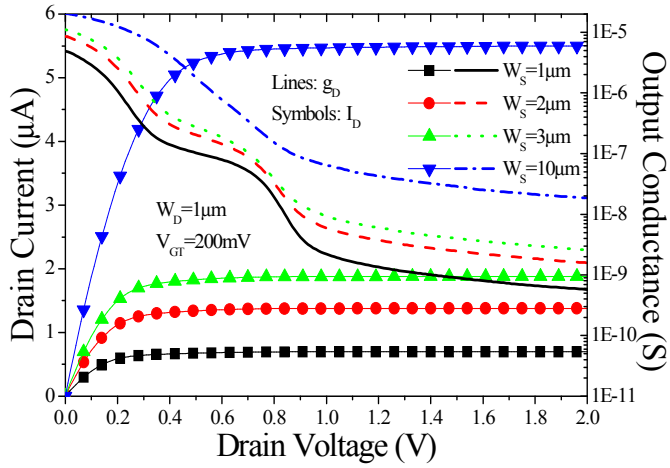

Fig. 9. Simulated drain current (left axis) and output conductance (right axis) as a function of the drain voltage for W_D=1µm varying W_S, extracted at V_{GT}=200mV.

for W_D=1µm varying W_S (A) and for W_S=1µm changing W_D (B), extracted at V_{GT}=200mV. It is verified from Fig. 11(B) that, besides the increase of the intermediate potential due to the increment of W_D (lower resistance of the M_D transistor), there is a lower variation of the intermediate potential with the drain voltage in the saturation regime, reducing the output conductance. Based on Fig. 11(A), with the increase of W_S, there is a reduction of the intermediate potential due to lower resistance of the M_S transistor. However, an increment of V_X variation with the drain voltage is observed in the saturation regime, which implies in higher output conductance.

Fig. 12 exhibits the transconductance (A), the output conductance (B), the intrinsic voltage gain ($A_V=g_m/g_D$) (C) and the Early voltage ($V_{EA}=I_D/g_D$) (D) as a function of W_D, extracted at V_{DS}=1.5V and V_{GT}=200mV. It is possible to notice that the increase of W_D promotes a slight increment of transconductance, increasing the intrinsic voltage gain and the Early voltage, since the presence of a wider M_D transistor considerably reduces the output conductance, but does not affect the drain current level. When W_S is incremented, the increase of output conductance is larger than the increase of

transconductance, reducing the intrinsic voltage gain and the Early voltage. Based on Fig. 9, it is possible to observe that the reduction of I_D caused by a narrower M_S transistor is less significant than the decrease of g_D, which explains the increase of V_{EA} with the reduction of W_S in Fig. 12(D). The maximum A_V and V_{EA} have been verified for the widest M_D transistor and narrowest M_S transistor. In [1], the maximum A_V for the SC configuration was 60dB when W_D=3W_S, whereas for the A-SC (W_S=1µm, W_D=3µm) structure a gain of 80dB was observed. Besides that, when W_S=W_D, one can note the same A_V=77dB, since the intermediate potential does not vary among these A-SC structures. This way, by increasing W_S=W_D, there is a proportional increment of g_m and g_D, obtaining the same A_V.

IV. Conclusions

This paper has studied the influence of the channel width of the M_S and M_D devices on the analog performance of the A-SC

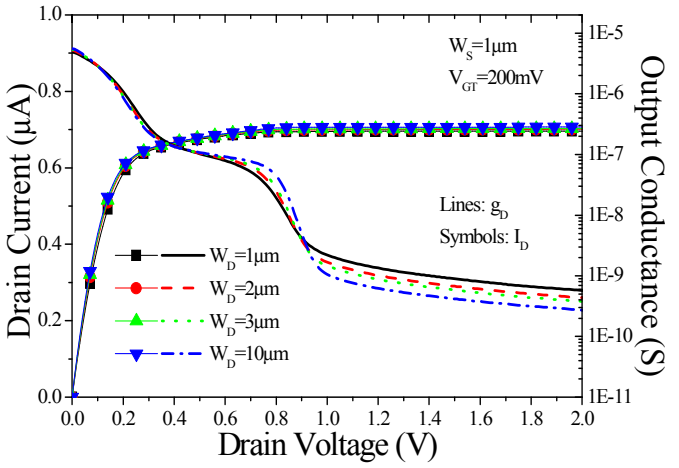

Fig. 10. Simulated drain current (left axis) and output conductance (right axis) as a function of the drain voltage for W_S=1µm varying W_D, extracted at V_{GT}=200mV.

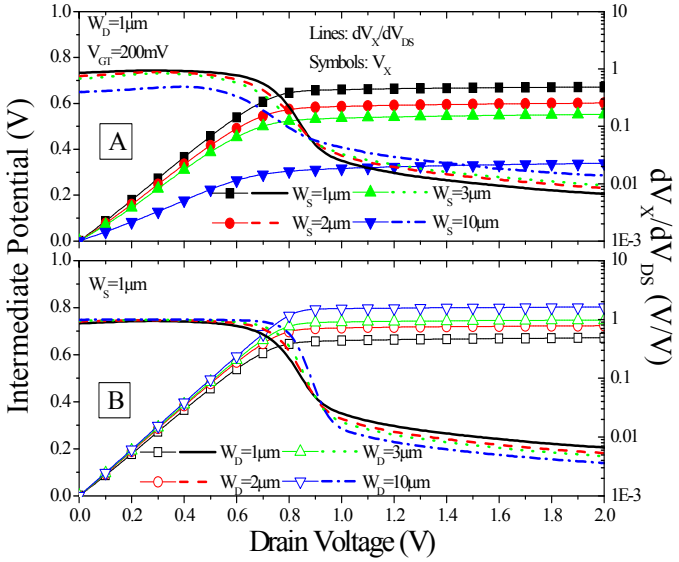

Fig. 11. Simulated intermediate potential (left axis) and dV_X/dV_{DS} (right axis) as a function of the drain voltage for W_D=1µm changing W_S (A) and for W_S=1µm varying W_D (B), extracted at V_{GT}=200mV.

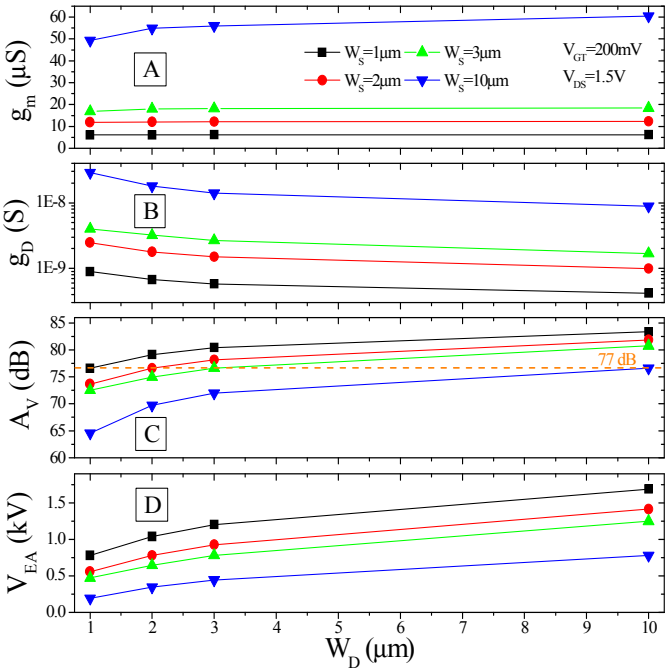

Fig. 12. Simulated transconductance (A), output conductance (B), intrinsic voltage gain (C) and Early voltage (D) as a function of W_D varying W_S, extracted at V_{DS}=1.5V and V_{GT}=200mV.

structure. It has been confirmed that the M_S device dominates the A-SC conduction for all V_{GS}. However, for high V_{GS}, the M_D transistor also impacts on the current flow. It has been noted that depending on the channel widths of the M_S and M_D transistors, there is a variation in V_X, affecting g_m and g_D. The increase of W_S has incremented g_m and g_D, reducing A_V and V_{EA}, whereas the increase of W_D has slightly increased g_m, but reduced g_D, thereby incrementing A_V and V_{EA} by a factor larger than 2, which is very significant. Summing up, the largest A_V and V_{EA} have been obtained for the A-SC structure composed by the narrowest M_S transistor and the widest M_D device.

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