Improving Noise and Linearity of CMOS Wideband Inductorless Balun LNAs for 10-GHz Software-Defined Radios in 28nm FDSOI

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***Abstract*— This paper presents the analysis and optimization of inductorless balun low-noise amplifiers (LNA) in a 28-nm fully-depleted SOI CMOS technology for wideband universal software-defined radio transceivers by means of an algorithm that optimizes the main figures of merit. An optimum combination of two techniques is provided leading to a new topology that overcomes the main tradeoffs of the previous circuits improving both linearity and noise with competitive bandwidth (BW), gain and power. Post-layout simulations show a BW of 10 GHz, a gain of 17 dB, an IIP3 of 7.4 dBm, and a NF of 3.4 dB with only 2.5 mW power consumption from a 1-V supply.**

Keywords—28-nm FDSOI CMOS integrated circuits; low-noise amplifiers; low-power electronics; linearity

I. Introduction

Next generation wireless communications requires the development of universal integrated radio transceivers for software-defined radio [1, 2]. A low-noise amplifier (LNA) covering the full spectrum, is a critical and highly demanding component as it must meet broadband input matching, high gain, low noise figure (NF) and low-power consumption.

Several wideband inductorless CMOS LNAs have been published [3-5] but they feature low linearity and, to the authors' knowledge, no low-power inductorless balun LNAs have been proposed for 10-GHz bandwidth (BW) operation. This paper analyses the potential performances of state-of-art inductorless balun LNAs for low power and low noise operation at 10 GHz when ported in a 28-nm FDSOI CMOS process. On another hand, experimental improved linearity performances of 28-nm FDSOI have been recently reported in [6]. To fairly exploit these features, we used a genetic algorithm to optimize the required figures of merit for all considered LNAs. Our study allows us to identify an optimum combination of techniques to get a new highly-linear wideband inductorless balun LNA topology with improved power, gain and NF. Post-layout simulations are provided for this topology.

II. State of Art LNAs Analysis and comparison

The standard CG-CS (Common Gate - Common Source) topology [7] has drawn significant attention for its noise-cancelling technique. A cascode transistor can be added to increase the gain while enhancing the BW [3]. A further optimization uses a feedback loop to increase the CG transconductance, and reduce noise, implemented as: (1) gate of the main CG transistor connected to the output of the CS stage to boost its transconductance [3]; (2) shunt negative capacitance at the input of the LNA to improve the wideband noise [7]; and (3) cross-coupled CG-CS LNA to mitigate the trade-offs between gain, impedance matching and noise [5].

To evaluate the performance of each structure all of them have been simulated in a 28-nm fully-depleted (FD) SOI CMOS technology and fed with a supply voltage of 1 V. The Non-dominated Sorting-based Genetic Algorithm II (NSGA-II) [8] has been used to optimize the different structures in order to compare their performance in a fair and efficient manner. The different LNAs have been optimized to get the lowest possible NF and power consumption holding gain higher than 14 dB and both 3-dB BW and input impedance BW (S_{11} below -10 dB) higher than 10 GHz. For linearity simulation, two-tone testing has also been performed for second and third-order inter-modulation distortions. Table I summarizes the comparisons results. Although all the mentioned alternatives improve some tradeoffs of the simple CG-CS LNA, linearity is still an issue to improve.

III. Optimum LNA Topology

In order to achieve a highly linear LNA with good gain, and noise performances, we propose to use, in combination with the cross-coupled structure, a new version of the derivative superposition technique [9]. It consists in the inclusion of an auxiliary PMOS transistor (M_4) operating in saturation but under different operation conditions from the main CS NMOS; in this way the third derivatives of the drain current from the main and auxiliary transistors are added to cancel distortion. Fig. 1 shows the LNA resulting from this multi-technique combination. An amplifying block that consists in a cascade common-source stage (M_2, M_3 and R_{L2}) to reduce the Miller effect due to C_{gd2}, and a feedback block that consists in the CG stage (M_1, R_{L1}, R_B) are used. To avoid the use of large, imprecise and narrow-band on-chip inductors, the biasing of the CG stage uses a resistor R_B at the expense of some voltage headroom. The auxiliary PMOS transistor (M_4) is used to improve linearity but also improves input impedance and gain without affecting the noise or BW, and with no significant increase of the power consumption.

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TABLE I.
PERFORMANCE COMPARISON OF THE DIFFERENT LNA TOPOLOGIES SIMULATED (SCHEMATIC LEVEL) IN 28 NM FDSOI CMOS TECHNOLOGY

Topology	Stand. CG-CS [7]	Cascode [3]	M_1 to V^-_{Out} [3]	Neg. Cap [4]	Cross-coupled [5]	PROPOSED
Power consumption (mW)	1.8	1.9	2.1	2.0	2.0	2.1
Bandwidth (GHz)	11.0	11.0	11.1	11.1	11.0	11.1
Gain (dB)	15.7	16.4	16.6	19.3	17.7	19.2
IIP3 (dBm) @ 1 GHz	4.2	7.5	-1.8	-21.3	1.31	12.1
Noise figure (dB) @ 1 GHz	3.1	3.2	2.8	2.9	2.8	2.2

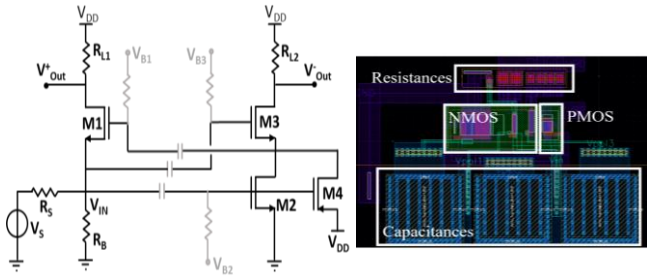

Fig. 1. Proposed low noise amplifier topology and layout (Area<35 µm x 26 µm including coupling capacitors).

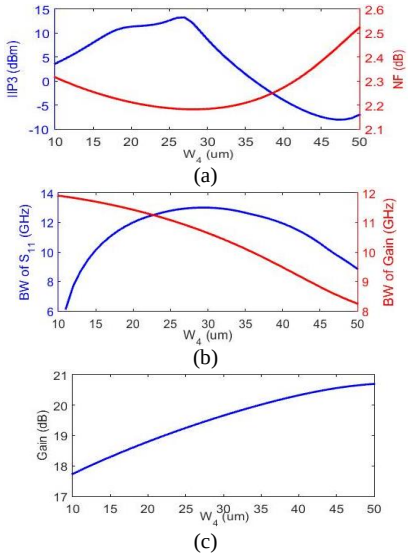

Fig. 2. Impact of PMOS transistor in the different parameters: (a) IIP3 and NF, (b) BW of S11 and BW of the gain and (c) Gain.

IV. RESULTS AND DISCUSSION

To validate the improvement of the optimum LNA with respect to previous inductorless balun LNAs, it has also been optimized in a 28-nm FDSOI technology at 1 V using the NSGA-II approach under the same conditions. Table I also benchmarks the proposed LNA results. It provides the best performance amongst all simulated ones thanks basically to a lower NF and a higher linearity for similar BW and power consumption. The effect of the added PMOS transistor is studied in Fig. 2. It can be seen that there is a large range of widths of the PMOS transistor which optimizes both IIP3, noise and input impedance bandwidth (i.e. S_{11} below -10 dB).

Post-layout simulations have also been carried out to better characterize the optimum inductorless LNA taking into account all the parasitic elements of the circuit. The layout is shown in Fig. 1. A new parametrization of the system was performed to achieve 10-GHz BW with post-layout simulations. The LNA shows 2.5-mW power consumption with 17-dB gain, 7.4-dBm IIP3 and 3.5-dB NF. These results appear better than the state of art balun LNA thanks to a lower power consumption with high linearity and low noise. Also the area is reduced thanks to the absence of inductors not scaling with technology.

V. CONCLUSIONS

This paper provides an analysis of inductorless balun LNAs for wideband universal software-defined radio transceiver exploiting the enhanced device properties of 28-nm FDSOI CMOS technology, thanks to a genetic optimization algorithm. After a first comparison of the state of art architectures, we identify an optimum combination of techniques to design a new low-power LNA topology for 10-GHz BW with improved linearity and NF without compromising power consumption.

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