Back-gate bias effect on UTBB-FDSOI non-linearity performance

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**Abstract**—This work investigates experimentally the non-linearities of FDSOI MOSFETs from DC to RF frequencies. The effect of the back-gate bias on non-linearity of the device is studied by means of 2nd and 3rd harmonic distortions (HD2 and HD3) extracted from dc I-V curves as well as from large-signal RF measurements using 1-dB and IP3 points. It is shown that the non-linearity is reduced by applying a positive back-gate bias. The reasons for this reduction are increasing of “effective body factor” and lesser mobility degradation with increase of the positive back-gate bias.

Keywords-component: Fully depleted (FD) SOI; MOSFETs; non-linearity; harmonic distortion; measurements

# Introduction

Ultra-thin body (UTB) and ultra-thin buried oxide (UTBB) technology used for fully depleted silicon-on-insulator (FD-SOI) transistors is widely recognized as a promising candidate to continue downscaling trends beyond 28 nm-node low power CMOS applications requested by ITRS ‎[1]. It is also an important node toward RF-digital integration for such applications as, e.g., 5G and Internet of Things (IoT). This technology has already demonstrated not only improved DC but also RF performances. This technology has already demonstrated its outstanding performance with respect to other counterparts in terms of variability ‎[2], electrostatic control and short channel effects ‎‎[3]-‎[5], parasitic capacitances and resistances ‎[6]-‎[8] as well as RF ‎[9] and analogue [10] figures of merit (FoM).

One of the most interesting features of this technology is the possibility of back-gate control schemes or double-gate (DG) configuration thanks to ultra-thin buried oxide (BOX). By combining this feature with a highly-doped layer underneath the BOX, so called ground-plane (GP), an architecture with dual gate is achievable by which both static and dynamic behaviors of the device are further controlled and improved ‎[11].

In this work, a 3-port configuration of 30nm High-k/Metal Gate (HKMG) UTBB FD SOI MOSFET is employed to investigate the effect of DC back-gate bias on the RF and non-linearity figures of merit. While the non-linearity of MOSFET is an intrinsic feature that is crucial for RF communication circuits, only few reports on the non-linearity behavior of scaled FDSOI exist. For example in [10], the non-linearity in FDSOI devices is compared to their bulk counterpart, but the work is limited to current-voltage measurements and their derivatives. The present work extends that study to include large-signal harmonic distortions extracted from RF measurements.

# Device and measurement description details

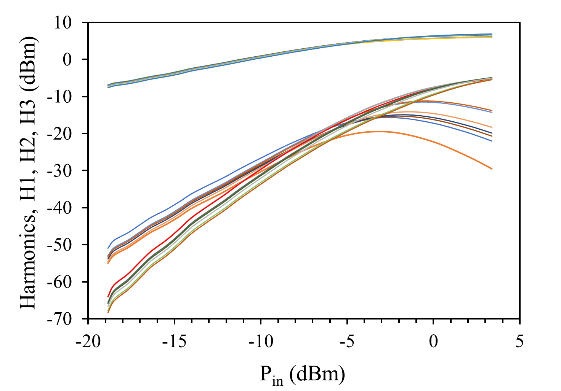
The studied UTBB FD-SOI nMOSFET is fabricated in the 28 nm FDSOI platform of ST-Microelectronics ‎[12]. BOX, Si body and equivalent gate oxide thickness are 25 nm, 7 nm and 1.3 nm respectively. The channel is rotated by 45° from the <100> plane. Studied device features 40 parallel fingers, 30 nm of length and 1 µm of width each.

For RF characterization the multi-finger device is designed and embedded in coplanar waveguide access pads. The common-source configuration design of the FD SOI nMOSFET provides the possibility of 3-port measurement in which the front-gate, drain and back-gate are referred to RF port1, 2 and 3 respectively. As shown in Fig. 1 illustrating the simplified cross section, the device layout features a particular access to the back-gate, so called flip-well architecture ‎[13], including a heavily doped n-type back plane located below the buried oxide (BOX) and an n-well which provides a natural substrate insulation between the devices.

De-embedding structures including open- and short-pads are implemented on the Si chip. Therefrom, in small-signal measurements the effects of interconnections on extrinsic capacitances and series resistances are withdrawn from S-parameters. In the large-signal measurements, the signal at the fundamental frequency of 900 MHz generated by an Agilent E8267D is amplified up to 4 dBm and injected into the DUT. The output signal is recorded and measured by an Agilent E4440A spectrum analyzer and an Agilent U2000B USB Power Sensor (with a frequency bandwidth of 10 MHz - 18 GHz). The recorded output signal contains the fundamental, 2nd and 3rd harmonics. The HD measurement is performed for various back-gate biases to observe its effect on non-linearity of the transistor (Fig. 2) by investigating of different key parameters e.g. 1-dB compression and third-order interception points which are discussed in next parts.

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Fig. 1. Simplified cross section of studied NMOS transistor with back-gate scheme.



H1

H2

H3

**Vbg = -0.3 … 3 V**

Fig. 2. Experimental Fundamental output (H1), 2nd (H2) and 3rd (H3) harmonics curves of studied FDSOI device at Vd = 1 V, constant Vg-Vth for various Vbg versus Pin.

# Non-linear results

## Static analysis

Fig. 3 shows gm1-Id curves of FDSOI device in saturation, at various Vbg where gm1=dId/dVg. As can be seen in Fig. 3, positive Vbg results in the reduction of gm1 maximum and global curve flattening. Similar trends are observed for higher order derivatives.

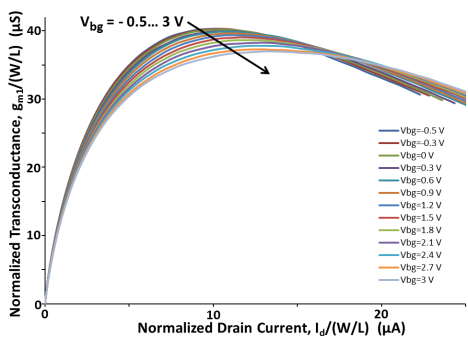


Fig. 3. Experimental gm1-Id curves of FDSOI device at various Vbg. L = 30 nm. W = 40 µm. Vd = 1 V.

Next to that, assuming a memoryless circuit excited by a sinusoidal signal with AC amplitude A, we calculated 2nd and 3rd order harmonic distortions as HD2=A/2|K2/K1|; HD3=A2/4|K3/K1| with Kn=1/n!.dnId/dVgn. It can be seen in Fig. 4 that HD2 minimum is shifted by Vbg to higher Id (and to lower Vg following Vth (Vbg) trend, not shown due to lack of space). Thus, depending on the regime (bias, current), HD2 can be considerably reduced. This is interesting from a design point of view. If one needs a certain current level, the better linearity can be achieved for that current by changing the Vbg. For example, Fig. 4 shows that 10-30 dB improvement can be obtained depending on the Vbg at given normalized current Id/(W/L) > 12 µA. In order to remove the effect of HD2 shift along the Id axis (due to Vth (Vbg) dependence) and visualize a pure effect of Vbg on HD2, Fig. 5 aligns HD2 minimums and plots HD2 as a function of Vg - Vg\_min HD2). Improvement of HD2 by Vbg is clearly seen. Similarly for HD3, one can see from Fig. 6 that there exists a current (and bias) range where HD3 can also be improved by the positive Vbg application (one can win about 3-5 dB).

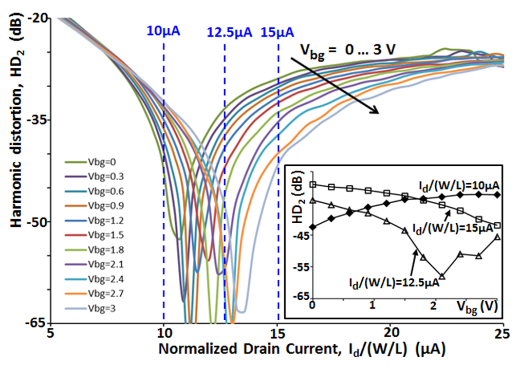


Fig. 4. Experimental HD2-Id curves of FDSOI device at various Vbg. Vd = 1 V. L = 30 nm. W = 40 µm. Insert gives HD2 vs. Vbg.

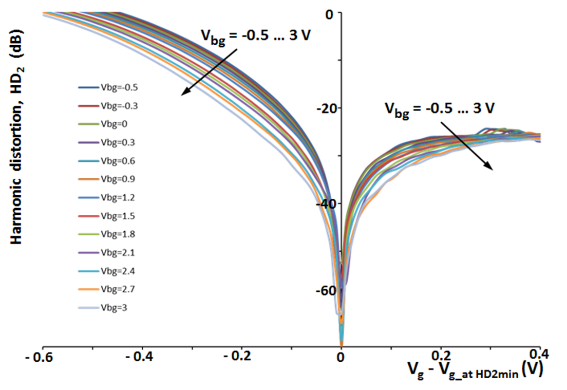


Fig. 5. Experimental HD2 as a function of Vg -Vg\_min HD2\_curves at various Vbg. Vd = 1V. L=30nm. W=40µm. Insert gives HD2 vs. Vbg.

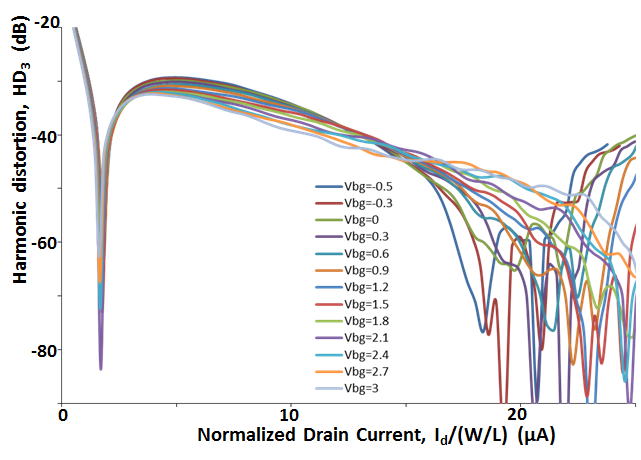


Fig. 6. Experimental HD3-Id curves of FDSOI device at various Vbg. Vd = 1 V. L = 30 nm. W = 40 µm.

Improvement of non-linearity with positive Vbg application can be related to higher "effective” body factor [14] and lesser vertical electric field mobility degradation.

## RF Figures of Merit

Fig. 7 illustrates extracted cut-off frequency fT values as a function of gate bias for various back-gate bias Vbg for the high and low drain biases (Vd = 1 V and Vd = 0.6 V, respectively). Maximum fT values as high as ~360 GHz are reached for the case of Vd = 1 V. These very high fT values are achievable thanks to the well-optimized (reduced) parasitic elements, as was studied in details in our previous work [15]. It is worth mentioning that even at low Vd of 0.6 V, the device features rather high maximum fT ~ 280 GHz which is beneficial for low voltage and low power applications. Next to that, it is worth pointing that application of positive Vbg results in a slight reduction of maximum achievable fT and in a shift of Vg at which the maximum is achieved to the lower values. Moreover, global fT vs. Vg curve flattens. Or in another words, one can say that the gate bias range where fT and fmax stay close to their peak values extends. These features are directly related to the above discussion on the gm\_max and gm versus Vg behavior as a function of Vbg (Fig. 2). Indeed, fT is directly proportional to gm.

Vbg = -0.3 … 3 V

Vd = 0.6 V

Vd = 1 V



Fig. 7. Experimental cut-off frequency fT curves versus front-gate bias Vg of studied FDSOI transistor for drain voltages of Vd = 0.6 V and 1 V at various Vbg.

## 1-dB compression and IP3 points

The transistor in common source configuration with an input large-signal at the gate introduces non-linearity in the output signal at the drain. Hence, in this mode, the output signal includes harmonics of the fundamental signal. The amount of non-linearity of a transistor in large-signal operation could be evaluated by two parameters, 1-dB compression point and third-order intercept point (TOI) as shown in Fig. 8. According to well-known theory, the 1-dB gain compression point (P-1dB) is defined as the power gain at which it lies 1 dB below the linear power gain in small-signal operation due to the non-linearities of the transistor. The dynamic range (DR) shown in Fig. 8 is the range where the transistor in amplifying mode has a linear power gain which is limited by the noise floor level [16]. In this range, the extrapolation of the fundamental and third-order nonlinearity curves (slope 1 and 3, respectively) will cross at a point called third-order intercept point (IP3). The IP3 usually refers to the input level and it is sometimes denoted IIP3 while the output level corresponding to the IP3 is presented as OIP3 [17]. When assessing the linearity of devices and systems, higher IP3 and 1-dB compression points are desirable. Below we show that the application of positive Vbg moves those points to higher values.



Fig. 8. Output power at 1-dB compression point and third order intercept point (IP3) versus input power on a logarithmic scale. The dynamic range (DR) is also shown.

Fig. 9 shows the input and output referred 1-dB compression point versus Vbg from -0.3 to 3 V at 900 MHz. The inset gives the output power, Pout and gain, G, versus input power, Pin at 1-dB compression point for different Vbg. The transistor is biased at Vd = 1 V and constant overdrive voltage (Vg-Vth) at which maximum gm is achieved. As can be observed in Fig. 9, by tuning Vbg to higher positive voltages, 1-dB compression point is shifted to higher (Pin, Pout) values showing more linearity of the device. By changing Vbg from -0.3 to 3 V, 1-dB compression point is improved by 1.2 dB extending linear DR of the device and thus making possible to get 1.2 dB more linear output power from the device. However, as illustrated in Fig. 9, at higher Vbg, the gain slightly decreases. This behavior is quite consistent with above discussion on the non-linearities extracted from I-V measurements i.e. obtaining lower peak-gm and flatter gm curves leading to lower gain and better linearity of the transistor. As shown in Fig. 3, the condition of maximum gm is achieved for normalized drain current Id / (W/L) of around 10 µA. As can be seen in Fig. 4 and 6, at this current (bias) condition, a degradation of HD2 and an improvement of HD3 by the positive Vbg is observed. The same trend is observable in RF measurement results shown in Fig. 2. The IP3 point is in correlation with HD3 which is expected to be improved.

The improvement of third-order intercept point (IP3) with increase of positive Vbg is shown in Fig. 10. It can be seen that by tuning of Vbg from 0 V to 3 V, OIP3 and IIP3 increase by about 1 and 1.25 dB, respectively.



Fig. 9. Input and output referred 1-dB compression point at Vd=1 V, constant over drive voltage Vg - Vth at maximum gm and 900 MHz versus Vbg from -0.3V up to 3 V. Insert gives the gain and output power vs. input power at 1-dB compression point for various Vbg.



Fig. 10. Input and output referred IP3 point at Vd=1 V and constant over drive voltage Vg - Vth at maximum gm for various Vbg from -0.3V up to 3 V.

# Conclusion

Non-linear behavior of 3-port FDSOI MOSFETs was studied through dc and RF experimental results. Effect of back-gate bias on non-linearity and RF FoMs was analyzed. Application of positive Vbg in FDSOI was shown to open a way for non-linearity reduction (providing e.g. 10-30dB win in HD2, 3-5dB in HD3, depending on bias/current conditions as well as output-referred 1-dB compression and IP3 points increase by 1.2 dB and 1 dB). Non-linearity behavior as a function of Vbg revealed by DC and RF measurements agree well. The reduction of non-linearity by the positive Vbg application can be understood in terms of “effective” body factor and mobility behaviors as a function of Vbg.

##### Acknowledgment

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