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Temperature dependence of frequency dispersion in III–V metal-oxide-semiconductor C-V and the capture/emission process of border traps

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This paper presents a detailed investigation of the temperature dependence of frequency dispersion observed in capacitance-voltage (C-V) measurements of III-V metal-oxide-semiconductor (MOS) devices. The dispersion in the accumulation region of the capacitance data is found to change from 4%–9% (per decade frequency) to ~0% when the temperature is reduced from 300 K to 4 K in a wide range of MOS capacitors with different gate dielectrics and III-V substrates. We show that such significant temperature dependence of C-V frequency dispersion cannot be due to the temperature dependence of channel electrostatics, i.e., carrier density and surface potential. We also show that the temperature dependence of frequency dispersion, and hence, the capture/emission process of border traps can be modeled by a combination of tunneling and a "temperature-activated" process described by a non-radiative multi-phonon model, instead of a widely believed single-step elastic tunneling process. © *2015 AIP Publishing LLC*.
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In case of III-V based Metal-Insulator-Semiconductor devices,[1] an issue which is gaining attention now is a significant amount of frequency dispersion commonly observed in the accumulation region of capacitance/conductance-voltage measurements[2–5,7–10] as shown in Fig. 1. Numerous reports on possible explanation of this phenomena using interface states,[2,4] disorder induced gap states (DIGS),[3,5] border traps (BTs)[7–10,14,15,25,28] have been published. While all these models are based on spatial displacement of charge from source (semiconductor channel) to defect states, the location of these defects and the nature of such charge-defect interaction are still under debate. In the framework of border traps, it has been shown in various reports[7–10,14,15,25,28,30] that the observed dispersion is due to the interaction of conduction band electrons with BTs, defects present in the dielectric but very close to the interface with the semiconductor. Some annealing techniques[4] have been reported to give promising results on reduction of such defects. But there is still a lack of agreeable understanding of the nature of interaction of defects with the charge carriers. A physical understanding of this interaction is not only required to be able to explain observations in electrical characterization and reliability measurements like C-V, hysteresis and Bias Temperature Instability (BTI) but also for developing an efficient technique to characterize these defects. In this paper, the BTs in III-V Metal-Oxide-Semiconductor capacitor (MOSCAP) devices are studied using AC capacitance-voltage (C-V) measurement technique with temperature as the parameter. Through temperature dependence of frequency dispersion in accumulation region of C-V, the nature of BT capture and emission process is investigated for MOSCAPs with different dielectrics and III–V channel materials.

It has been shown that frequency dispersion cannot be explained by either series resistance or interface states close to conduction band. In contrast, the time constant of border traps is large and distributed enough to explain both the dispersion in C-V data and flatness of G/ω-ω data in strong accumulation.[8,9]

It is proposed[7–10,13] that the border traps interact with channel electrons through tunneling due to their spatial

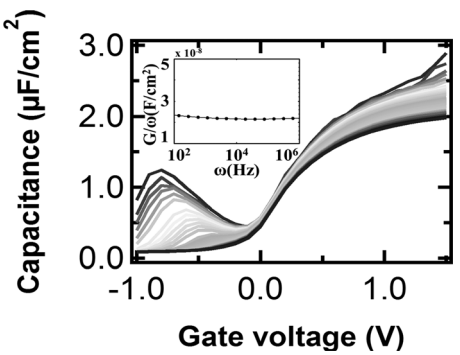

FIG. 1. Measured C-V (and G/ω-ω in inset) data of TiN/2 nm HfO_2/2 nm GdAlO/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor at 26 logarithmically spaced frequencies from 1 kHz to 1 MHz.

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separation with traps and the presence of an energy barrier due to the gate oxide. In addition, based on measurements done in a limited temperature range, it was concluded that BT capture/emission process is only weakly temperature dependent, a characteristic of an elastic process.[7,28] Needless to say, that all the characterization techniques that have been developed use this elastic process as the physical basis of their formulations.[2,3,5,6,8–10]

But reports on reliability measurements through BTI[11] and time dependent defect spectroscopy (TDDS)[12] of various high-k dielectrics suggest that the trap capture/emission in the oxide strongly depends on the temperature. Hence, a different physical mechanism for capture/emission, which is thermally activated, is used for analysis and characterization.

If both frequency dispersions in C-V and V_t shift in BTI measurements are due to defects in the high-k dielectric (although at relatively different distance from the interface), the physical mechanism for capture/emission in the two processes should be same. As the current focus of research on III-V devices shifts towards the defects in the high-k oxides, it is important, from the viewpoint of developing a physically correct characterization technique, to investigate the BT capture/emission process to point out the dominant mechanism. Therefore, it was the aim of this experiment to study the nature of capture/emission process of BTs using C-V measurements on III-V MOSCAPs in wider temperature range (4 K–300 K).

Various MOSCAPs were fabricated for the experiment as listed in Table I. One set of devices were processed on lattice matched 700 nm *n*-$In_{0.53}Ga_{0.47}As$ layer (2×10^{17} cm^{-3} doped) on InP (1×10^{18} cm^{-3} doped) substrate and another set on InP wafers without any InGaAs layer on top. Different dielectrics were deposited, in order to expand this study as listed in Table I, following the same procedure for pre-cleaning/treatment and same set of atomic layer deposition (ALD) precursors as used in Refs. 14 and 15. Circular TiN metal gate dots were then deposited by sputtering and patterned using lift off process. All the samples were annealed in forming gas (10% H_2) for 5 min at 400 °C. Capacitance–voltage (CV) and conductance–voltage (GV) measurements were carried out using a HP4284A LCR meter and a HP4294A impedance analyzer.

As a result of decrease in temperature from 300 K to 4 K, we observed that the frequency dispersion in strong accumulation region reduced significantly. This is shown in Fig. 2 for the C-V data of TiN/2 nm HfO_2/2 nm GdAlO/$In_{0.53}Ga_{0.47}As$ MOSCAP at 3 different ambient temperatures, 300 K, 77 K, and 4 K. It should be noted here that no

TABLE I. Split table of III-V MOSCAPs.

Sample ID	Dielectric	Substrate
A	3 nm $AlSiO_x$/2 nm HfO_2	$In_{0.53}Ga_{0.47}As$
B	2 nm $AlSiO_x$/2 nm HfO_2	$In_{0.53}Ga_{0.47}As$
C	2 nm Al_2O_3/2 nm HfO_2	$In_{0.53}Ga_{0.47}As$
D	2 nm ScAlO/2 nm HfO_2	$In_{0.53}Ga_{0.47}As$
E	2 nm GdAlO/2 nm HfO_2	InP
F	1 nm $AlSiO_x$/2 nm HfO_2	$In_{0.53}Ga_{0.47}As$
G	2 nm GdAlO/2 nm HfO_2	$In_{0.53}Ga_{0.47}As$
H	4 nm HfO_2	$In_{0.53}Ga_{0.47}As$

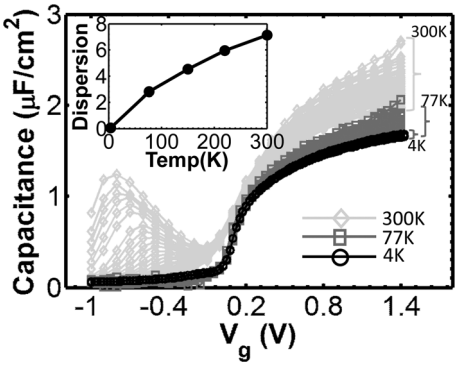

FIG. 2. Temperature dependence of frequency dispersion in measured C-V data at 26 frequencies (1 kHz–1 MHz) and 3 temperatures, 4 K, 77 K, and 300 K. Inset shows the quantitative depiction of this temperature dependence in the form of %dispersion.

carrier freeze-out was observed even at 4 K. It has been shown that devices based on significantly doped III-V material can avoid carrier freeze-out even at low temperatures.[16]

A significant decrease in dispersion in Fig. 2 clearly indicates that BT capture/emission is strongly temperature dependent. In order to get a better perspective on above dependence, frequency dispersion can be quantified by calculating percentage of dispersion per decade of frequency at a particular voltage in strong accumulation ($V_g = 1.2$ V) which is shown in the inset of Fig. 2. A significant decrease in dispersion from 7% at 300 K to almost no dispersion at 4 K clearly points to dominance of an inelastic capture/emission process in BT-charge carrier interaction, instead of a single-step elastic tunneling (ET) process.

To check if temperature dependent dispersion is specific to InGaAs substrate or a gate stack, the same experiment was repeated on MOSCAPs with 2 different substrates and various high-k dielectrics on top (refer Table I). The C-V measurements for samples C, D, E, and F were carried out between the temperature range of 77 K–300 K only but still show similar temperature dependent behavior as other samples. As shown in Fig. 3, we observed the same behavior for all the samples which indicates that, irrespective of the substrate or dielectric used, the underlying physical mechanism for temperature dependence of dispersion remains the same.

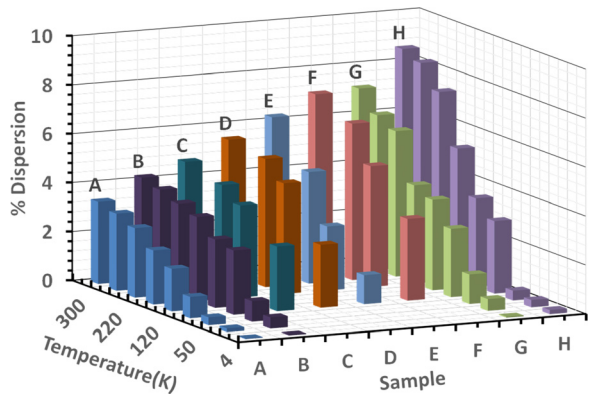

FIG. 3. Frequency dispersion at strong accumulation at different temperatures for all samples listed in Table I. The temperature dependency of frequency dispersion is observed for all the samples.

It should be noted that the dispersion values in case of different dielectrics (samples A-G in Table I) could be different because different effective field across the oxide could influence the capture/emission process. It could also be that ALD deposition of different dielectrics on different III-V substrate would result in different density or energy distribution of BTs. For the same dielectric stack on different substrates (samples F and H in Table I), the difference in absolute values of dispersion could be due to following reasons: First, a slight difference in the density of states in case of InP and InGaAs could change the overall time-constants of capture/emission which could affect dispersion. In addition, the underlying substrate can influence subsequent nucleation of dielectric layers in top. Thus, deposition of same stack on different substrate could result in different absolute border traps densities which, in turn, would mean different absolute frequency dispersion in C-V.

In the elastic tunneling model,[6] temperature dependence comes from electrostatics at the semiconductor interface: electron density, n_s, and surface potential, ψ_s. It is to be noted that in case of III–V based MOS devices biased in strong accumulation, the Fermi level, E_F, is well inside the conduction band, E_c. This means that, unlike the case in which the semiconductor is biased in the depletion region, the channel electrostatics is only weakly dependent on temperature in strong accumulation. An ideal C-V simulation, taking non-parabolic band effects in to account, was done for Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ without traps for validation as shown in Fig. 4.

A weak temperature-dependent channel electrostatics cannot explain such significant change in dispersion.[18,19] Our results indicate a presence of strongly temperature-dependent capture/emission process, in addition to tunneling. A temperature dependent capture/emission theory was postulated by Henry and Lang[17] for deep level traps in GaAs and InP, and Kirten and Uren[18] for Si:SiO_2 interfaces using random telegraph noise (RTN) data. Using an atomistic viewpoint, it was shown that capture/emission of an electron by a defect leads to a change in the distance between two atoms due to change in charge state of the defect, leading to a relaxation in the lattice structure around the defect.[17,19] This relaxation, represented as shift in an energy (E) vs configuration co-ordinate (q), creates a thermionic barrier between neutral and trapped states of the system. For the (electron + lattice) system to go from neutral state to trapped state or vice versa, as shown in Fig. 5, the barrier has to be crossed which leads to a strong temperature dependence of the trapping phenomenon.

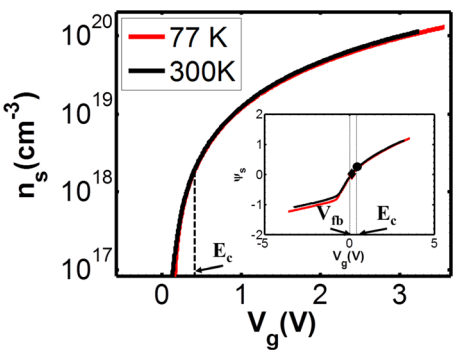

FIG. 4. Simulated temperature dependence of electron density, n_s, and surface potential, ψ_s (inset) at different gate voltages in strong accumulation.

In small signal analysis of MOS systems, trap capture/emission time constant is an important measure of capture/emission probability and trap response. In general, it is given by[6,8,18,19]

$$\tau = \frac{1}{n_s \sigma \upsilon_{th}}, \tag{1}$$

where σ is the trap cross-section, υ_{th} is the thermal velocity of the carriers, and n_s is the carrier concentration. The trap cross-section, σ, for elastic tunneling process is given by[6,8]

$$\sigma_{ET}(x) = \sigma_0 e^{2\kappa x}, \tag{2}$$

where σ_0 is the trap cross-section, x is the distance from the interface, and κ is the attenuation coefficient for an electron wave function decaying under an energy barrier, $E_{c,ox}$, given by $\kappa = \sqrt{2m^*(E_{c,ox} - E)}/\hbar$ where m* is the electron effective mass, E is the energy of electron wave function.

Much work has been done on mathematical formulation of Lattice relaxation based non-radiative multi-phonon (LR-NMP) model[17–22,25] but in order to reduce the complexity of our comparison with ET model, we have used the formulation proposed by Kirten and Uren[18] for trap time constant where trap cross section, in case of strong electron-phonon coupling approximation, is represented by Eq. (3)[18–20,31]

$$\sigma_{NMP}(x) = \sigma_n e^{-\frac{\Delta E_b}{KT}}, \tag{3}$$

$$\Delta E_b = \frac{\epsilon_R}{4} - \frac{(E_2 - E_1)}{2}, \tag{4}$$

where K is the Boltzmann constant, T is the temperature in °K, ΔE_b is the thermionic barrier height between neutral and trapped states, ξ_R is the lattice relaxation energy given by $Sh\omega_0$ where S is Huang Rhys factor, σ_n describes the overlap of the wave-functions of both states which reflects on the tunneling process and, within the WKB approximation, can be described by[18,20] $\sigma_n = \sigma_{0,NMP} e^{2\kappa x}$. For the calculation of

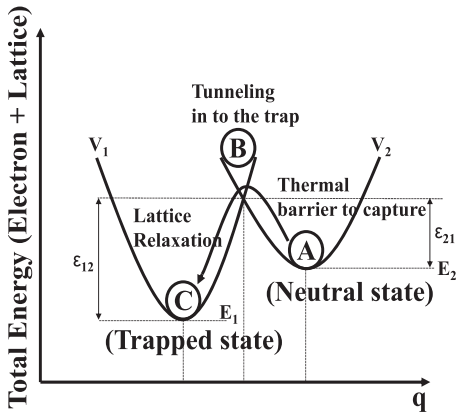

FIG. 5. A graphical representation of a temperature activated capture process involving tunneling (B). V_1 and V_2 represent the vibrational motion of the total system along a reaction coordinate. E_1 and E_2 are ground state energy of the total system in trapped (C) and neutral state (A), respectively. ε_{12} and ε_{21} are the thermal barriers for emission and capture, respectively.

ΔE_b, $\xi_R = 0.43$ eV and $E_{21} = 0.11$ eV have been used.[23,24] It should be noted that mathematical form of $\sigma_{0,NMP}$ could be different from σ_0 of Eq. (2) but it was chosen so that Eqs. (2) and (3) gives similar τ at the interface ($x = 0$). Assuming non-uniform distribution of defect density[25] and $\sigma_0 = 10^{-15}$ cm^2 in the oxide, we simulated the trap time constant for both ET and LR-NMP models as shown in Fig. 6. From Eqs. (3) and (4), it is evident that the temperature dependence is proportional to the height of thermionic barrier defined by the value of ΔE_b.[19,20,24] A small or negligible ΔE_b ($\Delta E_b \ll KT$) would result in a weak or negligible temperature dependence of BT capture emission. This can explain why some reported results[28] do not show as strong effect of temperature as in our work. It is possible that ALD deposition of Al_2O_3 on an InGaAs surface with different surface preparation or deposition methodology[28] leads to different defect type, density or distribution as compared to ex-situ surface treated samples as was done here, resulting in very small values of ΔE_b leading to a weak temperature dependent capture/emission process.

In order to simulate the effect of temperature on frequency dispersion and total admittance, based on ET and LR-NMP models, the simulated trap time constant values for different traps at various x and at different temperatures are then used in the equivalent circuit representation of distributed oxide trap model[8] given by following differential equation:[8]

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon_{ox}} + \frac{q^2 N_{bt} \ln(1 + j\omega\tau)}{\tau}, \tag{5}$$

where Y is the total admittance at distance x from the interface, ω is the AC frequency, N_{bt} is the trap density in cm^{-3}. Same non-uniform N_{bt} distribution[25] was used for simulation of both cases. Other parameters of the model were obtained by fitting[8] the simulation with measured data at T = 300 K. Simulation results, in Fig. 6, show that the temperature dependence is significantly stronger, in the case of LR-NMP than that of ET, which resembles closely with the experimental data. The close correlation of LR-NMP time constant with the values extracted previously[25] and dispersion simulation with measured data indicates the correctness of the hypothesis.

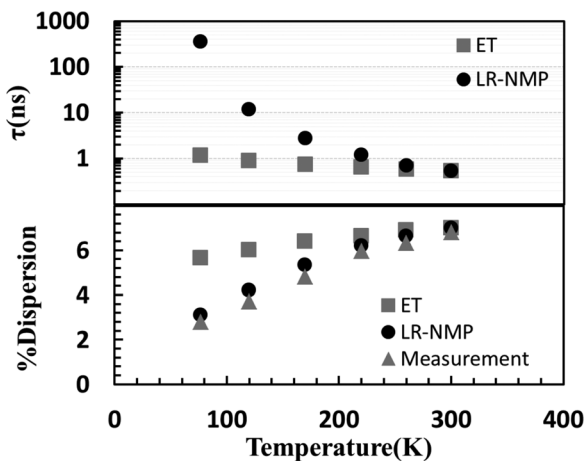

FIG. 6. Simulated temperature dependence comparison of trap time constant, τ, for a trap at a distance of 0.2 nm (for example) from the interface and %dispersion in total capacitance for elastic tunneling (ET) and LR-NMP model compared with measured data of Fig. 2.

Several reports based on different experimental techniques have shown the presence of a phonon assisted trapping in the high-k dielectrics. Inelastic electron tunneling spectroscopy (IETS) measurements[26,27,29] on HfO_2, Al_2O_3, and $LaAlO_3$ indicate the presence of various phonon modes corresponding to defects in such gate stacks, both on Si and III-V substrates. Leakage current[22,24] and random telegraph noise[30–32] measurements on high-k stacks have also been used to show the presence of such trapping mechanism, further corroborating the findings in this work.

In conclusion, we observed, in a wide range of III-V MOS capacitors, that frequency dispersion in the strong accumulation region is strongly temperature dependent. Also, our experimental results indicate that BT capture/emission is a 2-step process based on a multiplicative combination of a tunneling and "temperature-activated" process, described by a NMP model, instead of a single step direct tunneling process which is assumed to be the case currently. This temperature dependence of BT capture/emission conforms well to similar observations in reliability measurements like BTI and TDDS.

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