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RF SOI CMOS technology on 1st and 2nd generation trap-rich high resistivity SOI wafers

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ABSTRACT

In this work three different types of UNIBOND™ Silicon-on-Insulator (SOI) wafers including one standard HR-SOI and two types of trap-rich high resistivity HR-SOI substrates named enhanced signal integrity high resistivity silicon-on-insulator (eSI HR-SOI) provided by SOITEC are studied and compared. The DC and RF performances of these wafers are compared by means of passive and active devices such as coplanar waveguide (CPW) lines, crosstalk- and noise injection-structures as well as partially-depleted (PD) SOI MOSFETs. It is demonstrated that by employing enhanced signal integrity high resistivity silicon-on-insulator (eSI HR-SOI) compared to HR-SOI wafer, a reduction of 24 dB is measured on both generations of trap-rich HR-SOI for 2nd harmonics. Furthermore, it is shown that in eSI HR-SOI, digital substrate noise is effectively reduced compared with HR-SOI. Purely capacitive behavior of eSI HR-SOI is demonstrated by crosstalk structure. Reduction of self-heating effect in the trap-rich HR-SOI with thinner BOX is finally studied.

1. Introduction

During last decades, CMOS technology scaling-down has enabled millimeter wavelength operation and low-cost integration of digital, analog and RF systems on the same wafer for system-on-chip or system-in-package applications [1–3]. In this context, the most special advantage of SOI CMOS compared to bulk Si is the availability of high-resistivity silicon (HR-Si) substrate to achieve low crosstalk between passive and active devices and high-quality passive elements thanks to effective reduction of substrate coupling and losses in RF circuits [4,5]. However, HR-SOI substrate suffers from resistivity degradation due to the formation of parasitic surface conduction (PSC) beneath the buried oxide layer (BOX) [6–9] due to fixed oxide charges (Q_{ox}) within the oxide. One of the most efficient techniques to overcome this problem is to introduce a trap-rich layer at the Si/SiO_2 interface compatible with industrial SOI wafer production and thermal budget of standard CMOS process [8]. Such layer aims at capturing the free carriers forming the PSC and thus retaining the substrate nominal high resistivity. In this work two types of trap-rich HR-SOI wafers named 1st and 2nd generation of enhanced signal integrity (eSI HR-SOI) substrate having respectively a BOX thickness of 400 nm and 200 nm developed by Soitec are studied and compared with the classical HR-SOI substrate with a BOX thickness of 1 μm. One of the motivations of using trap-rich HR-SOI substrates with thinner BOX is the reduction of self-heating effect. Moreover, it creates a pathway for further ultimate BOX thinning used in advanced nano-scaled ultra-thin body and BOX (UTBB) fully depleted MOSFETs which allows threshold voltage control by means of back-gate biasing voltage V_{bg} [10]. Therefore, trap-rich HR-SOI with thinner BOX could be considered as a promising candidate.

2. Device description

In this work two types of trap-rich HR-SOI substrates denoted eSI Gen1 and eSI Gen2 as 1st and 2nd generations with 400 nm and 200 nm-thick BOX respectively and one standard HR-SOI with 1 μm BOX (all provided by Soitec) are characterized and compared for non-linearity effects, crosstalk, noise coupling, DC/RF figures of merit and self-heating. The test structure devices include

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0.52 μm-thick CPW lines and PD SOI nMOSFETs fabricated using TowerJazz 0.18 μm SOI CMOS process (Fig. 1).

The lateral dimensions of the CPW lines are 20, 18 and 100 μm for the central conductor, slot space and ground plane, respectively. The PD SOI nMOSFETs have 145 nm-thick active silicon film with a nominal operating voltage of 2.5 V. The studied RF body-tied MOSFET has a gate length (L_g) of 0.24 μm with 16 gate fingers of 2 μm each (W_f). The studied single-finger DC nMOSFET has a gate length (L_g) of 0.26 μm with 1.5 μm width (W_f). To investigate substrate coupling we used a passive crosstalk structure consisting of two identical metallic pads embedded into RF pads for probe measurement. Active crosstalk structure is used to study the propagation of a digital noise signal through the substrate [11]. This characterization is performed by measuring the frequency spectra at the nMOSFETs drain as the output port when a square noise signal is injected in the vicinity of the nMOSFET via a metallic RF pad with a certain distance from the transistor.

3. Transistor characteristics

3.1. DC and RF performance

The DC on-wafer measurements have been done using an Agilent B1500. As shown in Fig. 2, the drain current versus gate voltage (I_D-V_G) and transconductance vs gate voltage (g_m-V_G) curves in linear regime are almost identical for the DC transistor on the 3 different wafers. To eliminate the threshold voltage variations effect and fairly compare these results, g_m/I_D ratio versus $I_D/(W/L)$ curves for the same transistors are plotted in Fig. 3.

Fig. 3 shows that similar values of maximum $g_m/I_D \sim 31\ V^{-1}$ are obtained for all substrate types, as well as similar characteristics in strong inversion, with very slight deviations in weak inversion which could be related to CMOS process and measurements variability. From Figs. 2 and 3 it can be seen that neither the existence of trap-rich layer nor the BOX thickness affects the DC characteristics of the PD SOI MOSFETs.

High-frequency measurement of studied RF body-tied nMOSFET is performed to extract the current gain cutoff frequency (f_T) as one of the major RF figures of merit. f_T is known as unity current gain frequency at which the short circuit current gain (H_{21}) becomes unity (0 dB) [12–14]. RF measurements are done in the frequency range from 40 MHz up to 40 GHz using Anristu 37369A in combination with HP4145 semiconductor-parameter analyzer. By using the off-wafer line-reflect-match (LRM) calibration technique, the reference planes at the probe tips are determined. Then by means of on-wafer dedicated de-embedding structures, the unwanted parasitic effects introduced by the RF pads are removed. H_{21} is extracted from the measured S-parameters of the transistor in saturation regime at Vg bias corresponding to the maximum of g_m [15,16]. As shown in Fig. 4, cut-off frequencies f_T on all 3 wafers are almost the same.

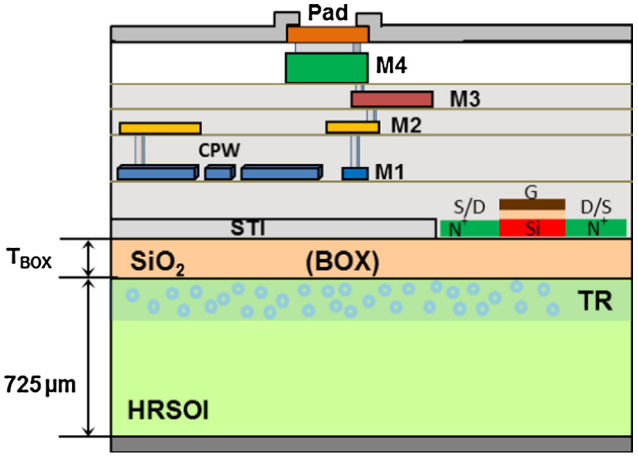

Fig. 1. Cross-section details of 4-metal layer 0.18 μm SOI CMOS process by Tower Jazz on top of high resistivity SOI substrates having different BOX thickness (T_{BOX}) provided by SOITEC.

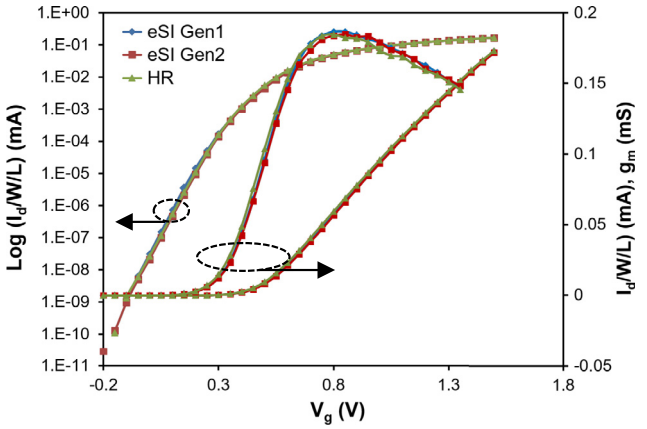

Fig. 2. Normalized I_d-V_g (linear and logarithmic) and g_m-V_g characteristics in linear regime (V_{DS} = 50 mV) of DC transistor for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

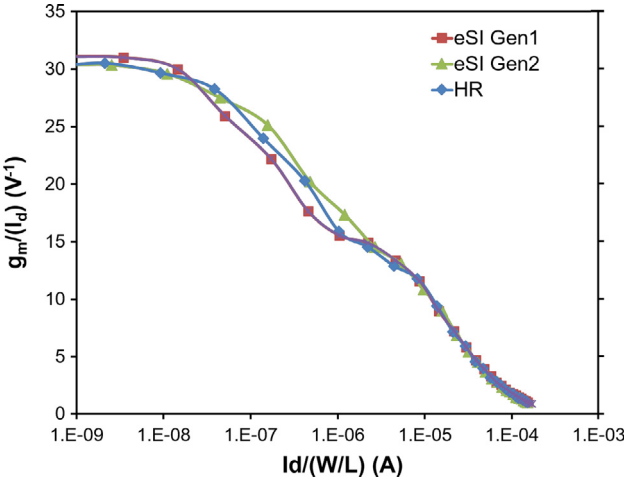

Fig. 3. g_m/I_d ratio versus $I_d/(W/L)$ DC transistor in linear regime (V_{DS} = 50 mV) on 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

According to the MOSFET small-signal equivalent circuit f_T can be in a first order expressed as [13,14,16]

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \tag{1}$$

where C_{gg} is the total gate capacitance (i.e. $C_{gs} + C_{gd}$). From Eq. (1), Fig. 4 and the results of DC measurements, it can be also concluded that total gate capacitances of PD MOSFETs fabricated on three different wafers are identical.

3.2. Self-heating and coupling through the substrate

Self-heating in SOI devices becomes a critical issue because of device downscaling and use of materials with low thermal conductivity like SiO_2 [17]. Thermal conductivity of SiO_2 (1.4 $W \cdot m^{-1} \cdot K^{-1}$)

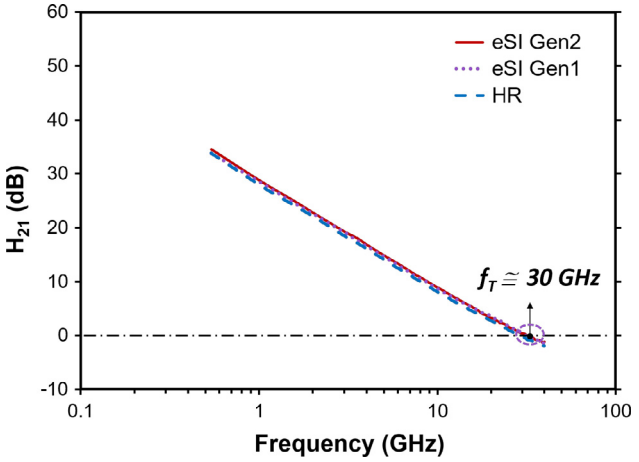

Fig. 4. Current gain cutoff frequency f_T at V_{DS} = 1.2 V and V_{GS} at which g_m (transconductance) is maximum for body-tied RF transistor for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

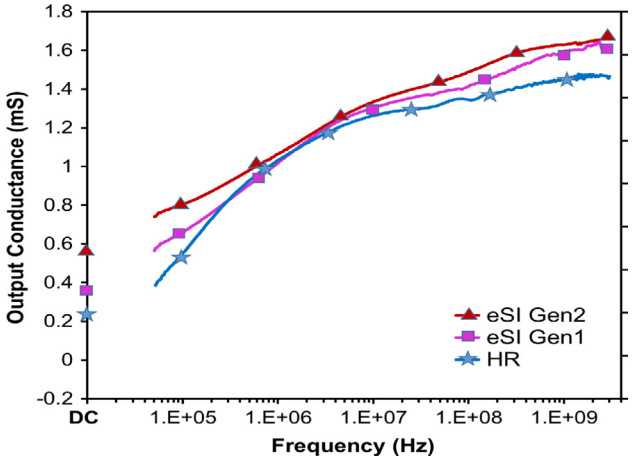

Fig. 5. Output conductance (g_{ds}) variation with frequency at V_{gs} = V_{ds} = 1.4 V.

is two orders of magnitude lower than that of Si (148 $W \cdot m^{-1} \cdot K^{-1}$) [18]. Consequently, the thicker the buried oxide layer (BOX) the higher the thermal resistance (R_{th}) of the device. In [19] it is shown that the thermal resistance is proportional to the square root of the BOX thickness. Therefore, BOX thinning is seen as a good solution for thermal properties improvement. Moreover, thin BOX enables other useful features in some advanced technology such as ultra-thin body ultra-thin BOX (UTBB) devices, notably threshold voltage control from the backgate [20–22] and better control of short channel effects [23].

In this section, the self-heating effect of studied RF body-tied PD nMOSFET is investigated by applying the RF technique [24]. In this technique, S-parameters are measured over a frequency range from 40 kHz up to 3 GHz at room temperature (25 °C), de-embedded using dedicated open structures and converted to Y-parameters. The output conductance g_{ds} is obtained from the real part of the Y_{22} parameter. In order to extract device thermal impedance from g_{ds} variation with frequency, hot chuck DC measurements are required. The output characteristics (I_d/V_{ds}) for different gate voltages (V_{gs}) at different temperatures were measured. The thermal resistance R_{th} is proportional to the g_{ds} transition amplitude and inversely proportional to the drain current temperature dependence [19,24]:

$$R_{th} = \frac{\Delta g_{ds}}{(V_{ds} g_{dT} + I_d)\partial I_d / \partial T_A} \quad (2)$$

where Δg_{ds} is the g_{ds} difference at low and high frequency (~50 MHz) and g_{dT} is g_{ds} at high frequency. $\partial I_d/\partial T_A$ is the dependence of drain current I_d on the ambient/chuck temperature T_A and can be extracted from I_d/V_{gs} or I_d/V_{ds} measurements at different temperatures. The average temperature rise ΔT is obtained from

$$\Delta T = R_{th} I_d V_{ds} \quad (3)$$

The studied devices are body-tied to prevent the floating-body or kink effect as a common feature in PD SOI devices causing the history effect [25]. Moreover, body-tied devices do not feature frequency variation of output conductance related to the floating-body and thus allow for more straightforward interpretation of output conductance frequency response in terms of self-heating and substrate effect and corresponding parameters extraction.

Fig. 5 shows g_{ds} variation with frequency when the transistor is biased in saturation regime (V_{gs} = V_{ds} = 1.4 V). DC output conductance values extracted from the I_dV_d measurements are also pointed. As discussed in [26–31], transitions in g_{ds} versus frequency curve are caused by various effects. The g_{ds} transition in tens of kHz to hundreds of MHz range is generally considered to be caused by self-heating [19,24,26–28]. As the frequency increases, device temperature stops following electrical oscillations and isothermal condition is reached [26]. As can be seen in Fig. 5, transistors on different substrates exhibit similar g_{ds} values at ~50 MHz where dynamic self-heating is removed, whereas at DC and low frequencies, HR substrate shows the lowest output conductance. This lowest output conductance in HR substrate case can be misleadingly interpreted as the better performance of devices on HR substrates. However, just contrarily, lower DC g_{ds} values obtained for the devices on HR substrate is a result of stronger self-heating caused by thicker BOX employed and thus worse performance can be expected.

Values of R_{th}, the average temperature rise ΔT in the device and the magnitude of g_{ds} transitions are plotted in Fig. 6. R_{th} and ΔT values are in line with previously measured values for other PD SOI devices [19,24]. As expected, R_{th} and ΔT are larger in devices with thicker BOX. In Fig. 5, the transition manifested in the GHz range (f_{sub}) is related to the substrate effect, which appears as a result of source and drain coupling through the substrate under the BOX [28]. As discussed in more details in [28,29,31], this

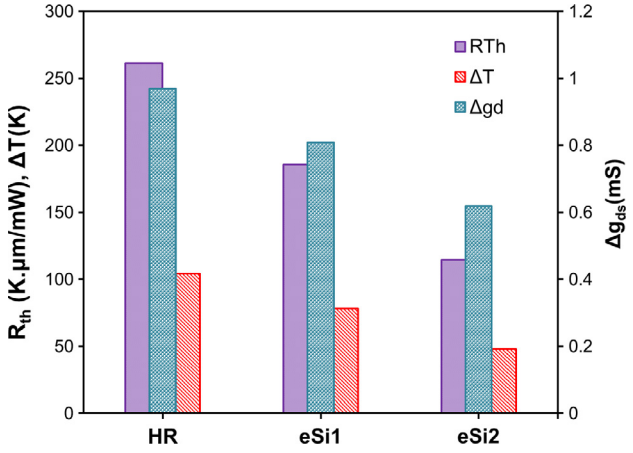

Fig. 6. Average temperature rise (ΔT), thermal resistance (R_{th}) and output conductance transition amplitude due to self-heating (Δg_{ds}) in studied body-tied RF transistors biased at V_{GS} = V_{DS} = 1.4 V for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

transition at high frequency can in a first order be modeled by the Si substrate resistance R_{Si} and its capacitance C_{Si}, when it can be considered as dielectric.

$$f_{sub} \sim \frac{1}{(R_{Si} \cdot C_{Si})} \tag{4}$$

It can be seen that the substrate-related transition (GHz range) shifts progressively to lower frequencies when HR substrate is replaced by eSI Gen1 and then by the eSI Gen2. This trend correlates with higher resistivity of eSI Gen1 and Gen2 discussed in next section (see Fig. 7). Indeed, characteristic frequency of this substrate transition was previously shown to be inversely proportional to the Si substrate resistance and capacitance [5,28,29,31] (see Eq. (4)). Furthermore, one can see that amplitude of substrate transition slightly increases in the case of eSI substrates Gen1 and Gen2. This is due to a stronger effect of parasitic source and drain coupling via the substrate in eSI Gen2/Gen1 devices due to the thinner BOX.

4. Substrate effective resistivity and harmonic distortion

The effective resistivity (ρ_{eff}) and total loss (α) on the 3 different types of substrate have been extracted by means of a 2100 μm-long CPW line S-parameters measurements [32]. On-wafer small- and large-signal measurements on CPW line are done based on a special setup [9] using an Agilent 4-port PNA-X vector network analyzer in the frequency range of 10 MHz up to 26.5 GHz. Fig. 7 shows that as stated before, due to the formation of PSC, the standard HR SOI substrate loses its nominal high resistivity and shows an effective resistivity of only 200 Ω·cm, whereas in 1st and 2nd generations of trap-rich eSI HR-SOI the substrate has kept its high resistivity of more than 2 kΩ·cm and 3 kΩ·cm, respectively, up to 5 GHz after CMOS processing. Another point that can be seen in this figure is that despite its thinner BOX, the eSI Gen2 HR-SOI substrate still shows a slightly higher ρ_{eff} and lower α compared to eSI Gen1 HR-SOI which could be explained by the higher nominal substrate resistivity in 2nd generation.

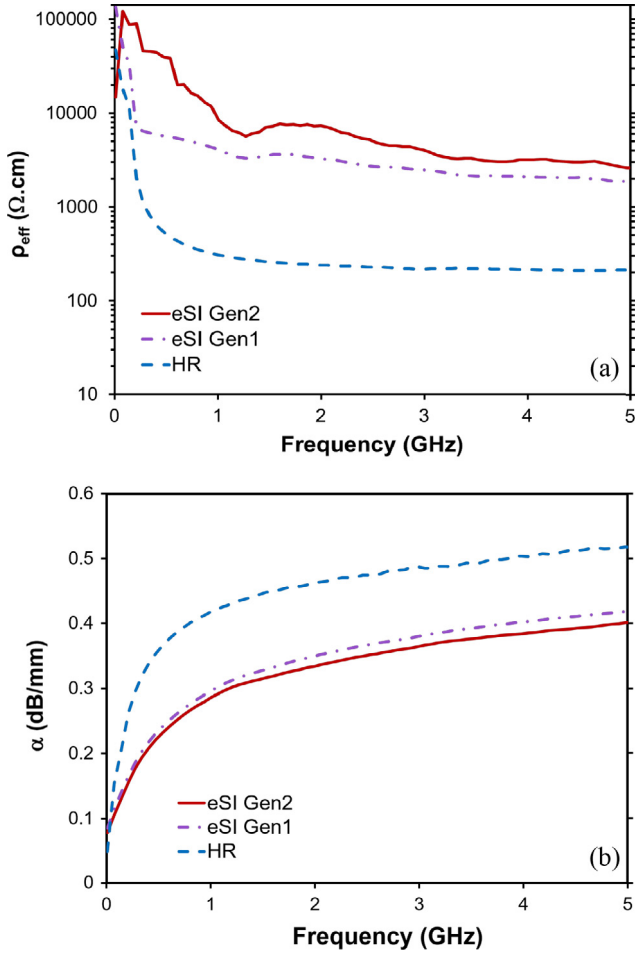

Fig. 7. (a) Effective resistivity. (b) Total Loss (Conductor and substrate) of 3 different substrates of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

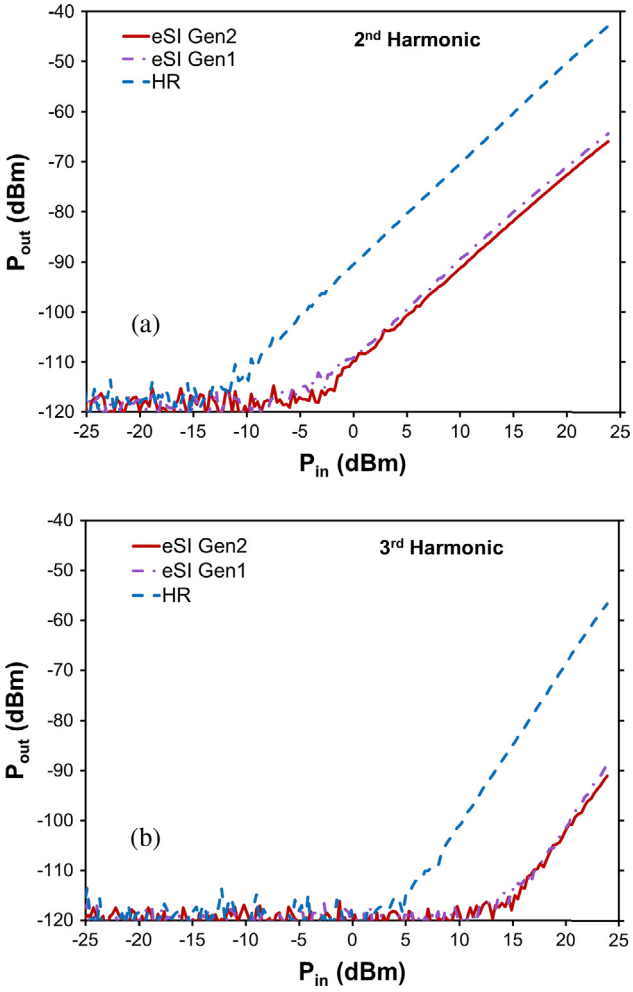

Fig. 8. (a) 2nd and (b) 3rd harmonic distortion measured at zero bias by CPW lines on 3 different wafers: 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

Fig. 8 illustrates the 2nd and 3rd harmonics distortion at the output of the CPW line on different wafers fed by a 900 MHz input RF signal for a power level ramp of −25 dBm up to 25 dBm and zero bias applied on the substrate. Compared to HR-SOI wafer, a reduction of 24 and 35 dB is measured on both generations of trap-rich eSI HR-SOI for 2nd and 3rd harmonics, respectively. From Figs. 8 and 7 it can be clearly seen that the level of the harmonics is inversely proportional to the substrate resistivity. This non-linear behavior can be explained by the PSC layer which changes the distribution of free carriers inside the substrate generating a modulated charge density at the Si/SiO_2 interface [33]. Consequently, the wafer becomes highly bias voltage dependent [34].

Fig. 9 demonstrates RF performance insensitivity of trap-rich eSI HR-SOI substrates to the applied bias voltages on CPW lines. It can be seen that under different bias conditions, the maximum variation of 2nd and 3rd harmonics distortion in HR-SOI wafer is much higher compared to trap-rich substrates.

5. Crosstalk analysis

For the RF system-on-chip (SoC) applications, less coupling through the substrate between devices fabricated on the same substrate, and therefore a good isolation between them, is desired [6]. In mixed-mode high-frequency integrated circuit in which RF analog circuits are integrated with baseband digital circuitry, the crosstalk coupling through the substrate is an important limiting factor especially for the analog part of the chip which is very sensitive to voltage variations on the power supply and substrate ground rails [5]. The strength of the coupling between different devices depends on device type (active or passive) and the characteristics of the substrate like effective resistivity, effective permittivity, BOX thickness, etc. [35]. Various methods are proposed in literature for reducing the coupling mechanisms between digital and analog parts through the common substrate like metal Faraday cages, guard ring, etc. [5,36–38]. In this work we use enhanced signal integrity high resistivity silicon on insulator substrates for this purpose. Indeed, a trap-rich layer at the SiO_2/Si-substrate will reduce the coupling between devices through the substrate and hence makes better isolation between them [6].

In this section the substrate crosstalk performances of different Silicon-On-Insulator (SOI) technologies including standard HR and two generations of trap-rich high resistivity eSI Gen1 and eSI Gen2 are comparatively investigated and compared. By this comparison the influence of substrate effective resistivity and buried oxide thickness (BOX) are analyzed. The study of crosstalk is demonstrated by two types of test structures: passive crosstalk structures and noise to active devices. The test structures have been designed and fabricated using TowerJazz 0.18 µm SOI CMOS process as stated in Section 2 on 3 different SOI wafers provided by Soitec.

The test structure is composed by two rectangles of metal 1 as the closest metal to the substrate with a length of 150 µm (L) and a width of 50 µm (W) representing the noise injector and the sensitive node as shown in Fig. 10. The two ports are separated by a distance S of 50 µm considered as the nominal structure for which the measurements and comparison between the 3 different substrates are shown.

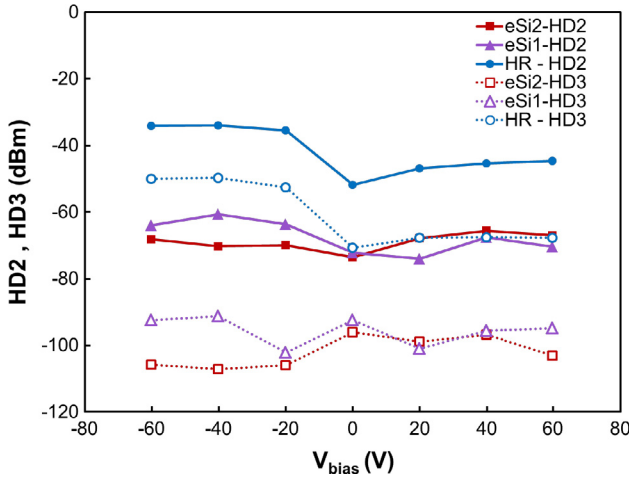

Fig. 9. The variation of 2nd harmonic distortion (HD2) and 3rd harmonic distortion (HD3) with bias changing from −60 V to +60 V at input power P_{in} = 20 dBm for 3 different wafers: 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

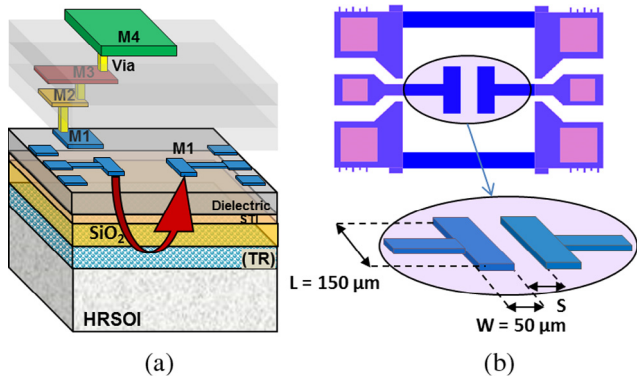

Fig. 10. Crosstalk structure in 0.18 µm TowerJazz CMOS process: (a) schematic; (b) top layout view.

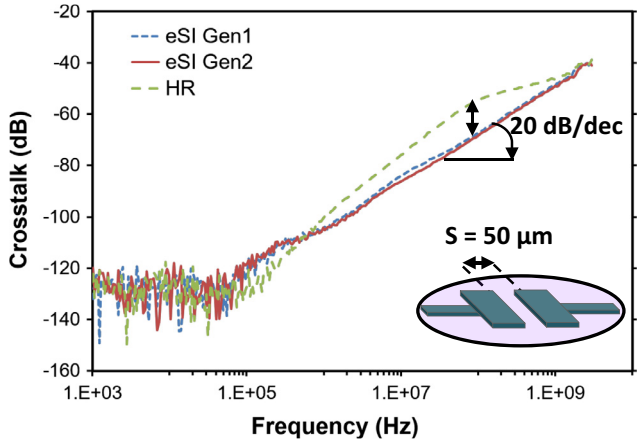

Fig. 11. Measured crosstalk versus frequency on HR-SOI, eSI Gen1 and eSI Gen2 HR-SOI substrates for a crosstalk structure with a pad distance of S = 50 µm and zero substrate bias.

By means of S-parameters measurements (S_{21}) of crosstalk structure shown in Fig. 10(b) with S = 50 µm in the frequency range of 1 kHz up to 3 GHz, the crosstalk level of different wafers is assessed and plotted in Fig. 11. As can be seen, a pure capacitive coupling is observed for both eSI Gen1 and Gen2 with a typical 20-dB/decade slope over the frequency range of 150 MHz-to-3 GHz. This behavior highlights the lossless property of the eSI HR-SOI substrates. Also a reduction of 15 dB of crosstalk is observed at 200 MHz for trap-rich HR-SOI wafers compared with conventional HR-SOI counterpart. From Fig. 11 it can be clearly seen that HR-SOI substrate suffers from higher crosstalk level (slope >20 dB/dec) due to the parasitic surface conduction (PSC) effect which is suppressed in eSI HR-SOI wafers [8,22,39,40].

The large-signal characterization of the crosstalk structure is illustrated in Fig. 12. It shows the 2nd (HD2) and 3rd (HD3) harmonics of 3 different wafers. The 2nd and 3rd harmonics are measured at the output of a crosstalk structure with a pad distance of S = 50 µm fed by an input RF signal at 900 MHz and for a power level ramp from −25 dBm up to 25 dBm. Fig. 12 illustrates that harmonics level of signals coupled through the substrate is reduced by 30 dB when HR-SOI substrate is replaced by an innovative trap-rich HR-SOI (eSI HR-SOI) one. This low harmonics level of −100 dB is comparable with insulating substrates like quartz [41,42].

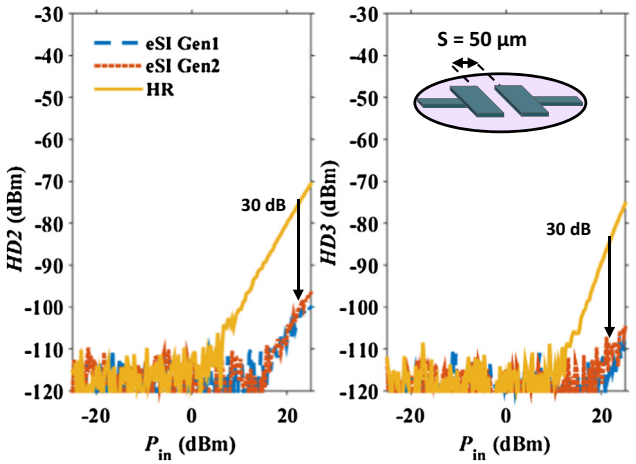

Fig. 12. Measured 2nd (HD2) and 3rd (HD3) harmonic distortions of a crosstalk structure with a pad distance of S = 50 µm and zero DC substrate bias.

Next to that, we study the harmful effect of the digital switching noise emulated by a clock signal, on the performance of an nMOSFET representing the analog/RF part in an RF SoC application [11]. To simulate such an environment, the test structure shown in Fig. 13 is implemented.

The test structure consists of a PD SOI nMOSFET located at a fixed distance of 350 µm from an RF metal pad used for injecting a digital noise signal to the structure. The PD SOI nMOSFET has a gate length, gate finger width and number of the finger of 0.24 µm, 2 µm and 64, respectively. It is biased in saturation (V_{GS} = 1.2 V and V_{DS} = 1.2 V). A fundamental input signal at 900 MHz is applied at the gate. A 5 V peak-to-peak digital noise source with selected frequencies of 50 kHz, 100 kHz, and 500 kHz, 1 MHz, 10 MHz, 50 MHz and 80 MHz is connected to the RF noise pad. Fig. 14 shows the coupled noise spectra at the MOSFET drain port for the three different substrates for the 10 MHz clock frequency when gate RF input signal is off. In HR-SOI substrate despite a thicker BOX of 1 µm compared to eSI HR-SOI wafers, the output peak noise level is 19.25 dB and

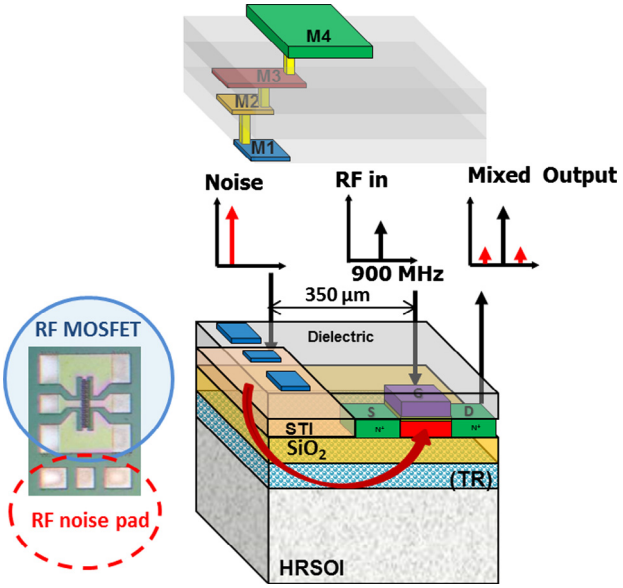

Fig. 13. Cross-section of PD SOI nMOSFET with a noise pad at a distance of 350 µm (center to center) lying on either eSI HR-SOI or HR-SOI wafers when a trap-rich layer exits or not respectively.

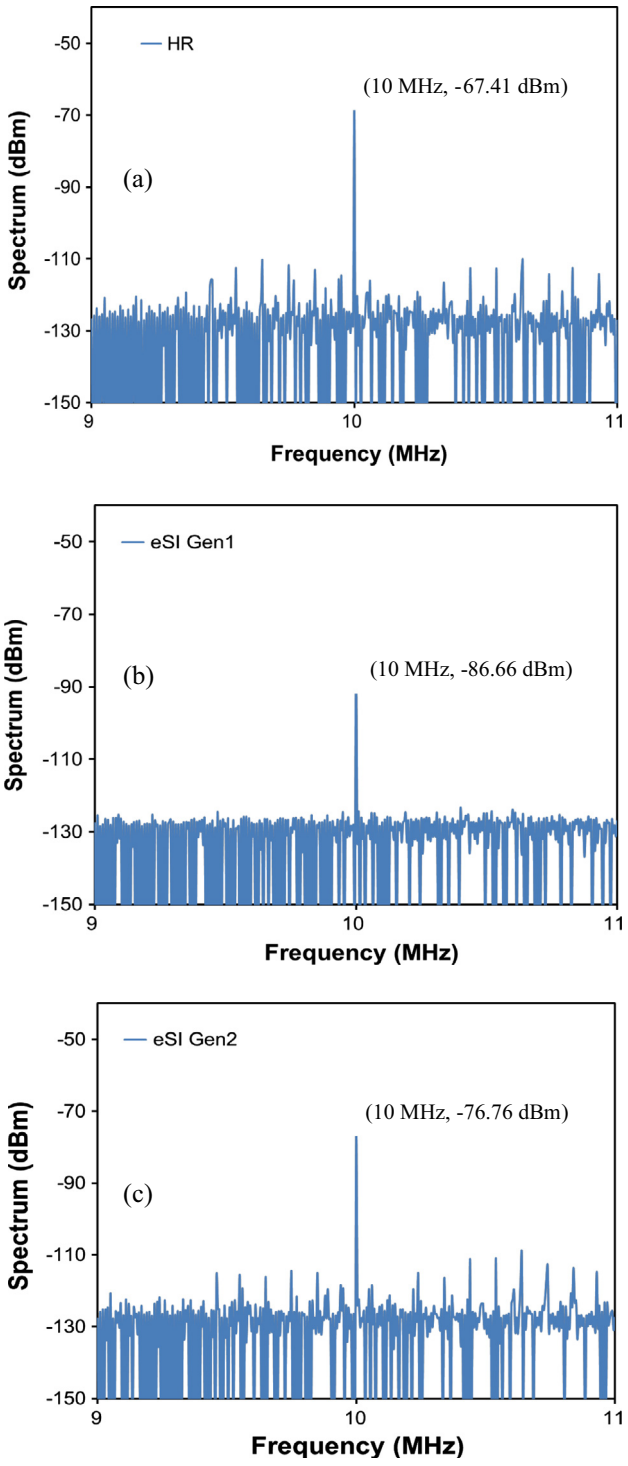

Fig. 14. Frequency spectrum of measured noise signal at the drain port of the PD nMOSFET having a gate length (L_g), gate finger width (W_f) and number of the finger (N_f) of 0.24 µm, 2 µm and 64 respectively biased in saturation with no fundamental RF signal at the gate. A digital noise signal (5 V peak-to-peaks at 10 MHz) is injected to the RF noise pad on (a) HR-SOI, (b) eSI Gen1 HR-SOI and (c) eSI Gen2 HR_SOI substrates.

9.35 dB higher than eSI Gen1 and eSI Gen2, respectively. This is due to the presence of highly parasitic conductive surface layer (PSC) at the BOX/HR-SOI interface by which a strong coupling and propagation of the noise signal is observed at the output. However, comparing Fig. 14(b) and (c), eSI Gen1 shows a noise coupling reduction of 10 dB compared to eSI Gen2 because of

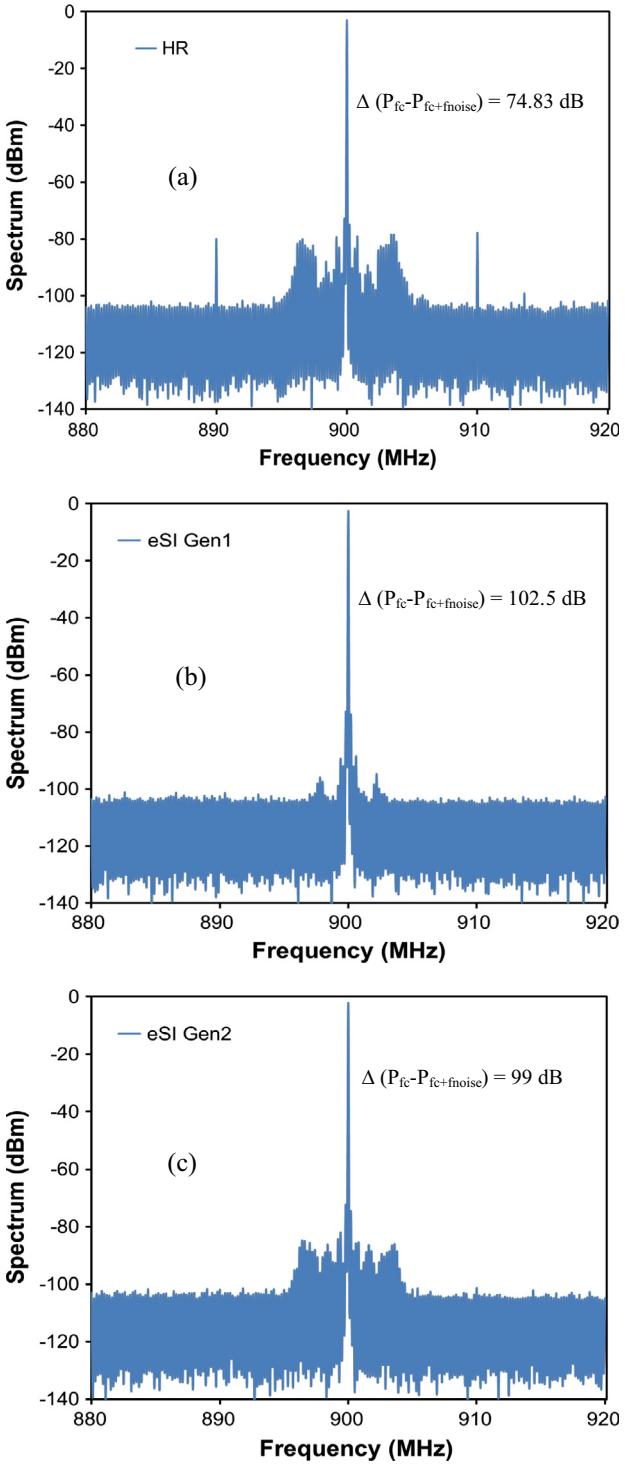

Fig. 15. Output spectrum of measured fundamental and noise signal at the drain port of the PD nMOSFET having a gate length (L_g), gate finger width (W_f) and number of the finger (N_f) of 0.24 μm, 2 μm and 64 respectively biased in saturation with a 900 MHz fundamental RF signal at the gate. A digital noise signal (5 V peak-to-peaks at 10 MHz) is injected to the RF noise pad on (a) HR-SOI, (b) eSI Gen1 HR-SOI and (c) eSI Gen2 HR_SOI substrates.

having a thicker BOX. Therefore, the 1st generation of trap-rich HR-SOI (eSI Gen1) shows a very good performance thanks to a good trade-off between substrate resistivity, from one side and a relatively "thick" BOX from another side.

When a fundamental RF signal with amplitude of A_{Fund} at the frequency of f_c is applied to the gate of the transistor, the digital

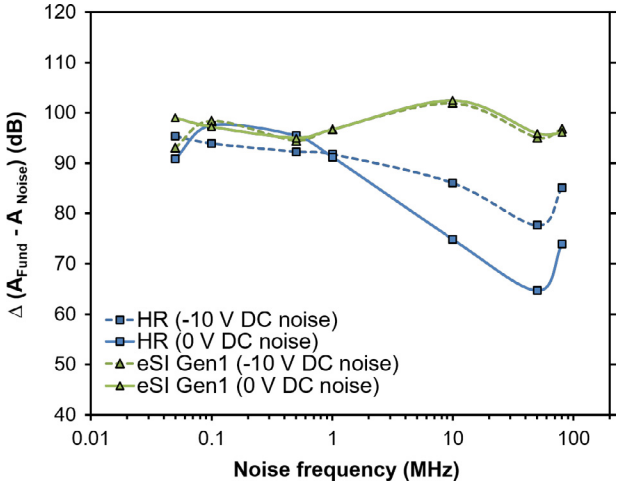

Fig. 16. Power level difference between 900 MHz fundamental RF input (A_{Fund}) and digital noise signal (A_{Noise}) on HR-SOI and eSI Gen1 substrates.

noise signal (A_{Noise}, f_{noise}) induces a mixing product and generates 2 N harmonics at $f_c - f_{noise}$ and $f_c + f_{noise}$. In this work, as illustrated in Fig. 15, the fundamental 900 MHz input signal and the square digital noise signal of 5 V peak-to-peak at f_{noise} = 10 MHz result in two harmonics at 890 MHz and 910 MHz. Fig. 15 evaluates the substrate performance through the parameter Δ defined as the power difference between the fundamental output signal and the harmonic ($P_{fc} - P_{fc+fnoise}$). The higher the Δ the better isolation will be achieved.

Fig. 15 shows an increase of Δ by 27.6 dB for eSI Gen1 and 24.2 dB on eSI Gen2 wafers compared with their HR-SOI substrate counterpart. Fig. 15 evidences that trap-rich eSI HR-SOI substrates filter well the digital noise signal from the output spectrum and show smoother response thanks to eliminating the effect of PSC at the BOX/HR-SOI interface, even though they have thinner BOX than HR-SOI. From Fig. 15(b) and (c), it can be clearly seen that 1st generation of trap-rich HR-SOI (eSI Gen1) shows a better trade-off between substrate resistivity and BOX thickness since most of the noise signals are suppressed. Fig. 16 demonstrates $\Delta = A_{fund} - A_{noise}$ measured at the drain pad of the transistor as the output when the injected digital noise signal changes from 50 kHz up to 80 MHz on HR-SOI and eSI-Gen1 (as the best substrate in our comparison).

A dc bias voltage of either 0 V or −10 V is also applied to the noise signal pad. By applying a negative dc bias voltage, the negative charges in PSC layer are repelled and a deep depletion will be formed. Therefore, it is expected that under these conditions, the coupled noise decreases and Δ increases. In Fig. 16 it can indeed be seen that application of negative dc bias voltage (−10 V) causes Δ increase by 11 dB at 10 MHz comparing to its level at 0 V bias in the case of HR-SOI substrate, whereas in the case of eSI Gen 1 it stays unchanged thanks to the traps that have frozen the free carriers in PSC. Moreover, from Fig. 16, one can see that in the lower frequency range below 1 MHz, since the carriers have enough time to relax, both HR-SOI and eSI HR-SOI substrates show similar behavior. In the frequency range higher than 1 MHz the effect of the traps is evident leading to almost constant high (w.r.t. HR-SOI) levels of Δ.

6. Conclusion

Use of a trap-rich layer underneath the BOX in HR SOI wafers allows the substrate to recover its high-resistivity properties and thus results in higher effective resistivity, lower losses, lower

crosstalk, lower harmonics level and hence higher linearity, all conserved after CMOS processing. It was shown that the presence of a trap-rich layer does not change the DC and RF characteristics of the MOSFET transistors. Moreover, with enhanced 2nd generation trap-rich eSI HR SOI substrate featuring thinner BOX of 200 nm, improved thermal properties can be achieved. Therefore, this technology is considered as a good candidate for SoC applications.

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References

[1] International Technology Roadmap for Semiconductor (ITRS), 2006 Edition.
[2] Buss D et al. SOC CMOS technology for personal internet products. IEEE Trans Electron Dev 2003;50(3):546–56.
[3] Benaissa K et al. RF CMOS on high-resistivity substrates for system-on-chip applications. IEEE Trans Electron Dev 2003;50(3):567–76.
[4] Vanada B. Study of floating body effect in SOI technology. Int J Mod Eng Res 2013;3:1817–24.
[5] Raskin J-P, Viviani A, Flandre D, Colinge J-P. Substrate crosstalk reduction using SOI technology. IEEE Trans Electron Dev 1997;44(12):2252–61.
[6] Ben Ali K, Roda Neve C, Gharsallah A, Raskin J-P. RF performance of SOI CMOS technology on commercial 200-mm enhanced signal integrity high resistivity SOI substrate. IEEE Trans Electron Dev 2014;61(3):722–8.
[7] Lederer D, Raskin J-P. New substrate passivation method dedicated to high resistivity SOI wafer fabrication with increase substrate resistivity. IEEE Electron Dev Lett 2005;26:805–7.
[8] Lederer D, Raskin J-P. RF performance of a commercial SOI technology transferred onto a passivated HR silicon substrate. IEEE Trans Electron Dev 2008;55(7):1664–71.
[9] Neve CR, Raskin J-P. RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates. IEEE Trans Electron Dev 2012;59(4):924–32.
[10] Makovejev S, Raskin J-P, Md Arshad MK, Flandre D, Olsen S, Andrieu F, et al. Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs. Solid State Electron 2012;71:93–100.
[11] Bol D, Ambroise R, Roda Neve CR, Raskin J-P, Flandre D. Wide-band simulation and characterization of digital substrate noise in SOI technology. In: IEEE international SOI conference, Indian Wells, CA. p. 133–4.
[12] Kazemi Esfeh B, Kilchytska V, Barral V, Planes N, Haond M, Flandre D, et al. Assessment of 28 nm UTBB FD-SOI technology platform for RF applications: figures of merit and effect of parasitic elements. Solid-State Electron 2016;117:130–7.
[13] Raskin J-P. Modeling, characterization and optimization of MOSFETs and passive elements for the synthesis of SOI MMICs. PhD thesis. Université catholique de Louvain; 1997.
[14] Colinge J-P, editor. FinFETs and other multi-gate transistors. Springer; 2008.
[15] Guo JC, Huang CH, Chan KT, Lien WY, Wu CM, Sun YC. 0.13 μm low voltage logic based RF CMOS technology with 115GHz f_T and 80 GHz f_{max}. In: Microwave conference, 2003. 33rd European, 4–6 October. p. 683–6.
[16] Kao HL et al. Limiting factors of RF performance improvement as down-scaling to 65-nm node MOSFETs. In: Korea-Japan microwave conference (KJMW), April 2009 (CGU).
[17] Makovejev S et al. Self-heating and substrate effects in ultra-thin body ultra-thin BOX devices. In: 2011, 12th international conference on ultimate integration on silicon (ULIS), Cork. p. 1–4.
[18] Pop E, Sinha S, Goodson KE. Heat generation and transport in nanometer-scale transistors. Proc IEEE 2006;94(8):1587–601.
[19] Jin W, Liu W, Fung SKH, Chan PCH, Hu C. SOI thermal impedance extraction methodology and its significance for circuit simulation. IEEE Trans Electron Dev 2001;48(4):730–6.
[20] Makovejev S, Kazemi Esfeh B, Barral V, Planes N, Haond M, Flandre D, et al. Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications. In: 2014, 15th international conference on ultimate integration on silicon (ULIS), Stockholm. p. 53–6.
[21] Noel J-P et al. Multi-VT UTBB FDSOI device architectures for low-power CMOS circuit. IEEE TED 2011:2473–82.
[22] Tsuchiya R, Horiuchi M, Kimura S, Yamaoka M, Kawahara T, Maegawa S, et al. Silicon on thin BOX: a new paradigm of the CMOSFET for low-power highperformance application featuring wide-range back-bias control. In: Proceedings of the international electron devices meeting. p. 631–4.
[23] Liu Q et al. Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond. In: Symp on VLSI technology; 2010. p. 61–2.
[24] Makovejev S, Olsen SH, Kilchytska V, Raskin J-P. Time and frequency domain characterization of transistor self-heating. IEEE TED 2013:1844–51.
[25] Colinge J-P. Silicon-on-insulator technology: materials to VLSI. 3rd ed. Kluwer Academic Publishers; 2004.
[26] Tenbroek BM et al. Self-heating effects in SOI MOSFET's and their measurement by small signal conductance techniques. IEEE Trans Electron Dev 1996;43:2240–8.
[27] Tenbroek BM et al. Impact of self-heating and thermal coupling on analog circuits in SOI CMOS. IEEE J Solid-State Circ 1998;33:1037–46.
[28] Kilchytska V, Levacq D, Lederer D, Raskin JP, Flandre D. Floating effective back-gate effect on the small-signal output conductance of SOI MOSFETs. IEEE Electron Dev Lett 2003;24(6):414–6.
[29] Kilchytska V, Levacq D, Lederer D, Pailloncy G, Raskin JP, Flandre D. Substrate effect on the output conductance frequency response of SOI MOSFETs. In: Hall S, Nazarov AN, Lysenko VS, editors. Nanoscaled semiconductor-on-insulator structures and devices. Springer; 2007. p. 221–38.
[30] Tenbroek BM et al. Identification of thermal and electrical time constants in SOI MOSFETs from small signal measurements. In: Proc 23rd ESSDERC. p. 189–92.
[31] Kilchytska V et al. Frequency variation of the small-signal output conductance of decananometer MOSFETs due to substrate crosstalk. IEEE Electron Dev Lett 2007;28(5):419–21.
[32] Lederer D, Raskin J-P. Effective resistivity of fully-processed SOI substrates. Solid-State Electron 2005;49(3):491–6.
[33] Kerr DC, Gering JM, McKay T, Carroll MS, Neve CR, Raskin J-P. The effect of a SiO_2 interface on RF harmonic distortion in CPW lines on silicon or passivated silicon. In: Proc 8th topical meeting silicon monolithic integr circuits RF syst, Orlando, FL, USA, January. p. 151–4.
[34] Lederer D, Raskin J-P. Bias effects on RF passive structures in HR Si substrates. In: Proc IEEE 6th topical meeting silicon monolithic integr circuits RF syst, San Diego, CA, USA, January. p. 334–7.
[35] Afzali-Kusha A, Nagata M, Verghese NK, Allstot DJ. Substrate noise coupling in SoC design: modeling, avoidance and validation. Proc IEEE 2012;94(12):2109–38.
[36] Stefanou S, Hamel JS, Baine P, Armstrong BM, Gamble HS, Kraft M, et al. Ultralow silicon substrate noise crosstalk using metal faraday cages in an SOI technology. IEEE Trans Electron Dev 2004;51(3):486–91.
[37] Juardar K. A simple approach to modeling crosstalk in integrated circuits. IEEE J Solid-State Circ 1994;29(10):1212–9.
[38] Blalack T, Leclercq Y, Yue CP. On-chip RF isolation techniques. In: Proc Bip/BiCMOS circuits technol meeting, Monterey, CA, USA; 2002. p. 205–11.
[39] Wu Y, Gamble HS, Armstrong BM, Fusco VF, Stewart JAC. SiO_2 interface layer effects on microwave loss of high-resistivity CPW lines. IEEE Microw Guided Wave Lett 1999;9(1):10–2.
[40] Schollhorn C, Zhao W, Morschbach M, Kasper E. Attenuation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon. IEEE Trans Electron Dev 2003;50(3):740–6.
[41] Raskin J-P, Desbonnets E. High resistivity SOI wafer for mainstream RF system-on-chip. In: 2015 IEEE 15th topical meeting on silicon monolithic integrated circuits in RF systems (SiRF), San Diego, CA; 2015. p. 33–6.
[42] Raskin J-P. High resistivity SOI wafer for mainstream RF system-on-chip. In: 2014 12th IEEE international conference on solid-state and integrated circuit technology (ICSICT), Guilin; 2014. p. 1–4.