Efficient passive energy harvesters at 950 MHz and 2.45 GHz for 100 µW applications in 65 nm CMOS

Pierre-Antoine Haddad, Jean-Pierre Raskin and Denis Flandre
Department of Electrical Engineering
Institute of Information and Communication Technologies, Electronics and Applied Mathematics,
Université catholique de Louvain, Louvain-La-Neuve, 1348, Belgium
Email: {pierre-antoine.haddad, jean-pierre.raskin, denis.flandre}@uclouvain.be

***Abstract*—Two 2-stage rectifiers are designed at 950 MHz and 2.45 GHz in 65 nm CMOS bulk technology to provide a 100 µW output power under 1 V with 79.9% and 76.6% power conversion efficiency, respectively. A portable and automated design methodology is used here based on foundry models. This methodology is extended to optimize both the cross-coupled and differential-drive rectifier architectures at UHF by using a derivative-free optimization algorithm. Transistor and capacitance sizing are discussed based on the method results and a simple RC-filter model. A first-order matching network is used to simulate the overall conversion efficiency of an energy-harvesting system using a 50 Ω antenna. For 100 µW output power, minimum input powers of -8.84 dBm and -8.56 dBm are simulated at 950 MHz and 2.45 GHz, respectively. These low power and high-efficiency AC/DC power converters can be used as energy harvesters in RF links to power wearable biomedical devices.**

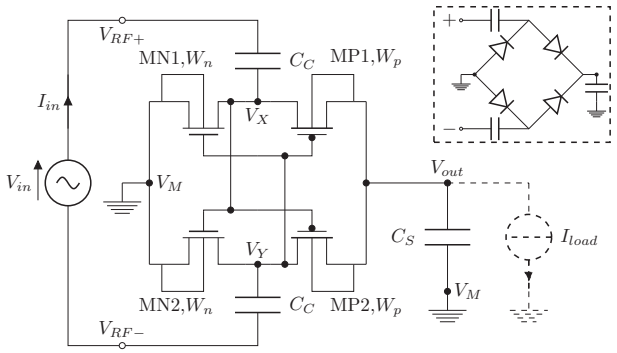

Fig. 1. Circuit of the single-stage differential-drive rectifier based on the full-wave bridge rectifier in inset.

I. Introduction

Preventive medicine will rely on implantable or wearable biomedical devices. As part of the Internet-of-Things (IoT) vision, wireless autonomous sensor nodes could be attached to patients to monitor their health. A practical and energy-sustainable implementation of this vision requires ultra low power (ULP) sensors and microcontrollers [1] powered by integrated micropower energy harvesters and high-efficiency power converters [2].

As our target application we consider a biomedical sensor system requiring 100 µW of power under 1 V and supplied by nearby electro-magnetic radiation sources at 950 MHz or 2.45 GHz. Both frequencies are investigated as the target application could interact with portable devices as smartphones for supplying power and retrieving the sensor measurements. Wireless systems operating in the 100 µW or less harvested power range require high AC to DC power conversion efficiencies (PCE) as this determines their maximum operating distance from the source. This has become a serious bottleneck in implementing power-hungry intelligent sensors with limited energy storage capabilities [3].

To rectify the input AC voltage signal and elevate the output DC supply value, passive AC/DC converters consisting of cascaded diodes and capacitors are typically used. Various architectures have been proposed to achieve ultra low power operation and CMOS integration with high PCE : the Full-Wave Bridge rectifier (FWB), the Greinacher/Cockcroft-Walton rectifier [4], the cross-coupled (CC) [5] and the differential-drive (DD) [6] rectifiers based on the FWB circuit topology. The DD architecture is shown in Fig. 1 compared to the FWB. When removing the coupling capacitors C_C and connecting directly V_X to V_{RF+} and V_Y to V_{RF-}, the DD architecture yields the CC architecture. Instead of diode-connected MOSFETs used in the FWB, the MOSFET gates in CC and DD are connected to nodes with a higher voltage swing to increase diode switching effectiveness.

Optimization of the transistors and capacitors design in these architectures has been discussed using an analytical approach in [3]. Design trade-offs are provided as well as design rules to improve power efficiency of the DD rectifier, but [3] does not provide a straightforward and automated way to reach the optimal design. The accuracy of the method in [3] also depends on the complexity of the analytical model used for the computation and is not necessarily easily portable.

In this paper we present the following contributions:

1) an automated design methodology using foundry models to design the transistors and reach the optimal PCE point of both CC and DD rectifier architectures given a target load current (Section II). The methodology avoids discontinuities at UHF by using a derivative-free optimization algorithm.
2) a discussion of the role of capacitors C_C and C_S and the design of their capacitance values (Section II).
3) two simulated designs of 2-stage rectifiers in 65 nm CMOS matched to a 50 Ω antenna, delivering 100 µW output power at 2.45 GHz and 950 MHz, respectively (Section III).

Section IV concludes with a comparison of the performances obtained with those reported in literature.

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II. Rectifier Design Methodology

The input voltage V_{in} considered to explain the methodology in this section is a 0.675 V peak amplitude sinusoid at 2.45 GHz. The target output load is a 100 µA DC current source (I_{load}). Circuit steady state is reached after 2 µs in the SPICE transient simulations used to compute the PCE that is retrieved by MATLAB during optimization. Power conversion efficiency for a rectifier is defined in steady state conditions by (1), where T is the period of source V_{in}. The n-stage voltage conversion efficiency (VCE) is defined as VCE $= V_{out,DC}/V_{out,DC,ideal}$, where $V_{out,DC,ideal} = n \max|\, V_{RF,+} - V_{RF,-}\,| = nV_{in,peak}$.

$$\text{PCE} = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{T}\int_0^T V_{out}(t)\,dt \cdot I_{load}}{\frac{1}{T}\int_0^T V_{in}(t)\cdot I_{in}(t)\,dt} \qquad (1)$$

A. Transistor design

To avoid leakage due to the parasitic junction diodes the transistor body nodes in Fig. 1 are connected to node V_M for NMOSFETs and node V_{out} for PMOSFETs [6]. The PCE of a single-stage Greinacher rectifier is shown in [4] to be a concave function of the diode transistor sizes. Similarly, using circuit symmetry, the PCE of the CC rectifier is also shown in Fig. 2 to be a concave function of NMOS transistor widths W_n and PMOS transistor widths W_p as defined in Fig. 1. The trade-offs leading to this concave function in the CC and DD architectures turn out to be comparable to those of the Greinacher architecture and are discussed in Section II-C.
The same gradient-based optimization method is applicable as a consequence. However, as seen in Fig. 2, the function is slightly discontinuous due to the parasitic capacitance abrupt changes here associated with the obligatory use of an integer number of MOSFETs with fixed maximum width. Hence, the Greinacher rectifier design methodology presented in [4] is modified to use a derivative-free optimization (Nelder-Mead simplex method) and is applied to maximize the objective function PCE(W_n,W_p) for a single stage. Optimization of transistor lengths L has in addition also been considered. For the initial widths optimization, the minimal length L_{min} for each transistor type was chosen to reduce channel resistive voltage drop. The lengths (L_n,L_p) were thereafter optimized separately using the same algorithm. Widths and lengths were then iteratively optimized until convergence was achieved.

B. Capacitance design

Using the effective resistances for the two MOS transistors, an RC filter model equivalent to the DD rectifier is shown in Fig. 3 to highlight the different roles of capacitors C_C and C_S.

Coupling capacitances C_C have a high-pass filtering role as is observed in Fig. 4 (top) for a single-stage DD rectifier as a threshold value for capacitance exists below which the AC signal cannot couple to the transistors. The value $C_C = 10\,\text{pF}$ is shown to be a good choice considering both PCE and VCE. This role of C_C is moreover confirmed by replacing this capacitance by a wire leading to the CC architecture. Optimization of the CC rectifier stage is thus equivalent to optimizing the DD rectifier when the coupling capacitance values C_C are appropriately chosen.

Output capacitance C_S is associated with low-pass filtering and output voltage ripple attenuation as shown in Fig. 4 (bottom) for a single-stage CC rectifier with identical transistor sizes. The value $C_S = 10\,\text{pF}$ is again shown to be a good choice at 2.45 GHz when considering output voltage ripple.

The objective at the target frequency is to reduce the ripple on each capacitor to avoid useless charge transfers resulting

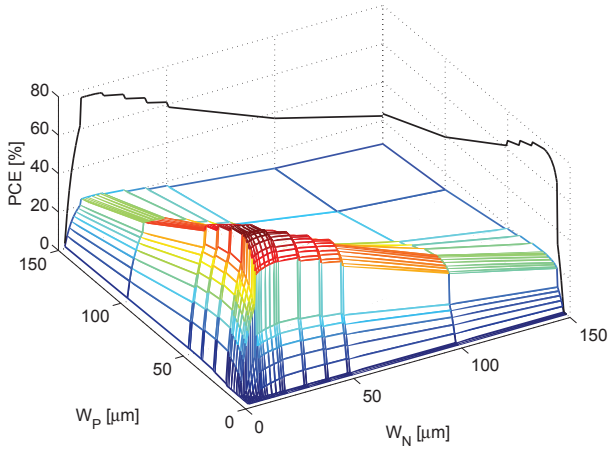

Fig. 2. Simulated PCE of the single-stage cross-coupled rectifier under a 100 µA load as a function of transistor widths W_n and W_p at 2.45 GHz for a 1.35 V_{pp} input voltage. Negative PCE values due to fixed I_{load} were forced to 0 for clarity. The curve is projected on both side-planes as black lines.

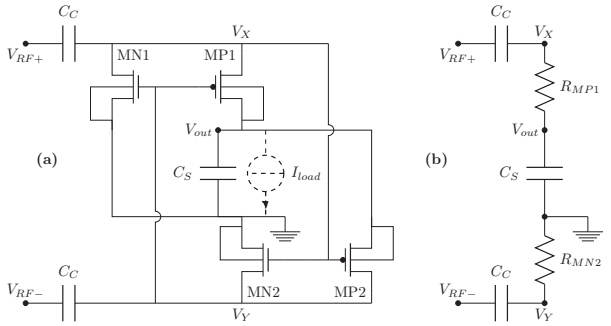

Fig. 3. Single-stage DD rectifier (a) modeled as an RC filter (b).

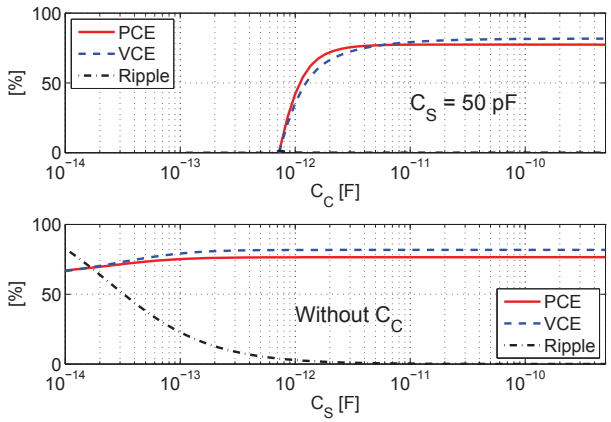

Fig. 4. Simulated behavior of the single-stage DD rectifier under a 100 µA load as a function of capacitance C_C at 2.45 GHz for a 1.35 V_{pp} input voltage (top). The behavior of the same DD rectifier without C_C (equivalent single-stage CC rectifier) is then simulated as a function of capacitance C_S (bottom). The peak-to-peak ripple is normalized with respect to the DC output voltage.

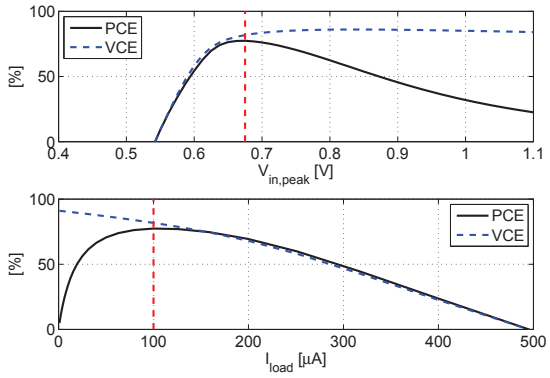

Fig. 5. Simulated PCE of the single-stage CC rectifier optimized for a 0.675 V_{peak} input voltage and a 100 µA load current at 2.45 GHz.

TABLE I. PERFORMANCE OF DESIGNED SINGLE-STAGE RECTIFIERS

Frequency	W_n	L_n	W_p	L_p	$V_{th,n/p}$	PCE	V_{out}	C_S
MHz	µm	nm	µm	nm	mV	%	mV	pF
950	12.77	79.5	20.35	60	522/-517	79.9	553	50
2450	13.85	67.5	19.99	60	522/-517	76.6	537	25

in PCE degradation. Lowering the cut-off frequencies of both filters by choosing sufficient capacitance values ensures proper circuit operation. To avoid effects of MIM capacitors process variability on circuit operation, values $C_C = C_S = 25\,\text{pF}$ were chosen for the 2.45 GHz circuit simulations in section III.

For multiple-stage rectifiers the role of C_C capacitors is essential as for each stage in operation, nodes V_X and V_Y will charge up to a common mode voltage with respect to their V_M and V_{out} nodes as shown in [6]. If all stages have their V_X and V_Y nodes respectively connected together at V_{RF+} and V_{RF-}, no voltage multiplication is observed. The C_C capacitors allowing DC decoupling of the cascaded stages must at least be used from the second stage on as in Fig. 7. If DC decoupling from the antenna is necessary, the first stage should be equipped with these capacitors as well.

C. Discussion

The PCE of the single-stage rectifier designed at 2.45 GHz in this section is shown in Fig. 5 as a function of V_{in} (top) and of I_{load} (bottom). After transistor widths, lengths and capacitance optimization by the method, and for the appropriate choice of threshold voltages, the peak PCE is shown to match the target input voltage $V_{in} = 0.675\,V_{\text{peak}}$ and load current $I_{load} = 100\,\mu\text{A}$. Table I shows that differences in the MOSFETs characteristics are automatically compensated by the method, resulting in different W_p and W_n values.

Given the MOS overdrive voltages associated with the fixed input voltage conditions, the widths and lengths optimization process adjusts the current-carrying capacity of the transistors and adapts it to provide the target load current. Hence, for smaller overdrive voltage conditions (i.e. for $V_{in} < 0.675\,V$) the transistors are thus undersized compared to the same load current and this reduces the PCE as seen in Fig. 5 (top) and results in a high startup voltage. Conversely, the transistors are oversized compared to the high overdrive voltages applied for $V_{in} > 0.675\,V$ and the ensuing high leakage reduces the PCE.

The physical reasons for the PCE concavity observed in Fig. 2 thus arise from the existing tradeoff between increasing the forward currents (favoring a high W/L) and diminishing the parasitic capacitance currents and reverse leakage currents (favoring a low W/L) for all transistors as discussed in [4].

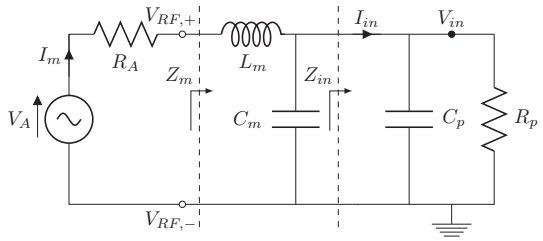

Fig. 6. Equivalent parallel resistance and capacitance model of the rectifier used to obtain the C_m and L_m values of the matching network.

III. RECTIFIER MATCHED TO AN ANTENNA

The rectifier PCE results presented in the previous sections were obtained based on a pure monochromatic sinusoidal input wave produced by the voltage source V_{in} from Fig. 1, without any source resistance. To assess whether these high conversion efficiencies could be maintained when coupling the rectifier circuits to an antenna, a hybrid CC/DD 2-stage rectifier was matched to an antenna with unit gain and real impedance $R_A = 50\,\Omega$. The rectifier used the parameters of table I to reach the target 1 V output voltage. The first-order LC matching network used is shown in Fig. 6 and Fig. 7.

The values for lumped capacitance C_m and lumped inductance L_m given in table II were determined based on an analysis of the transfer function $H = V_{in}/V_A$ of Fig. 6. The rectifier is modeled by input resistance R_p in parallel with capacitance C_p. Using a phasor representation, the input impedance of the matching network can be written as

$$Z_m = \frac{R_p}{1 + j\omega R_p(C_m + C_p)}\left[1 + j\omega\frac{L}{R_p} - \omega^2 L_m(C_m + C_p)\right]$$

where matching is obtained for $Z_m = R_A$. The matching frequency is obtained by canceling the imaginary part of Z_m and yields the relation $R_A = \frac{L_m}{R_p(C_m+C_p)}$. The following expressions for C_m and L_m are then obtained

$$C_m = \frac{1}{\omega_0 R_p}\sqrt{\frac{R_p}{R_A} - 1} - C_p \qquad L_m = \frac{\sqrt{R_A \cdot (R_p - R_A)}}{\omega_0}$$

where ω_0 is the target frequency to be matched. As seen from these expressions, existence conditions arise as C_m and L_m must both be real and positive values. Hence, this matching network cannot be used to match any rectifier.

The values of R_p and C_p are iteratively recomputed for the matched rectifier to fine-tune the values of L_m and C_m. The linear approximation model of the rectifier (using impedance Z_{in}) yields Z_m values close to R_A but not exactly equal due to the overall non-linear behavior and higher-order harmonics present at node V_{in} in Fig 6. Hence, the complex reflection coefficient $\Gamma = (Z_m - R_A)/(Z_m + R_A)$ resulting from the matching network has to be taken into account when computing the overall system efficiency PCE_{sys}.

$$\text{PCE}_{sys} = \frac{P_{out}}{P_{ant}} = \frac{P_{out}}{P_{in,m}}\left(1 - |\,\Gamma\,|^2\right) \qquad (2)$$

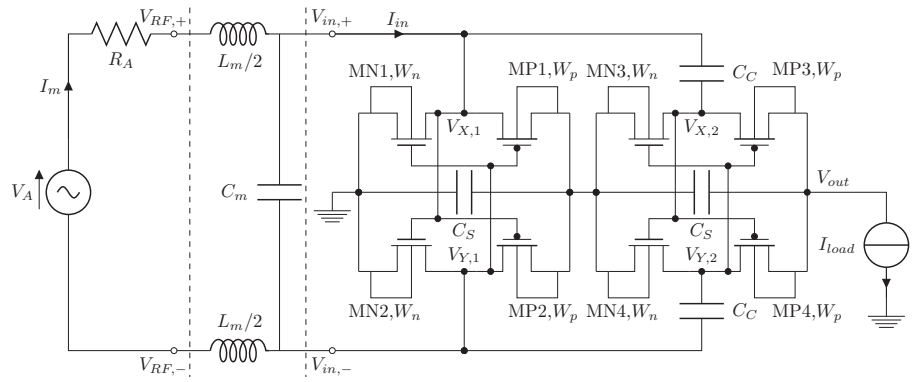

Fig. 7. Hybrid CC/DD 2-stage rectifier matched with a first-order LC matching network to an antenna of real impedance value $R_A = 50\,\Omega$.

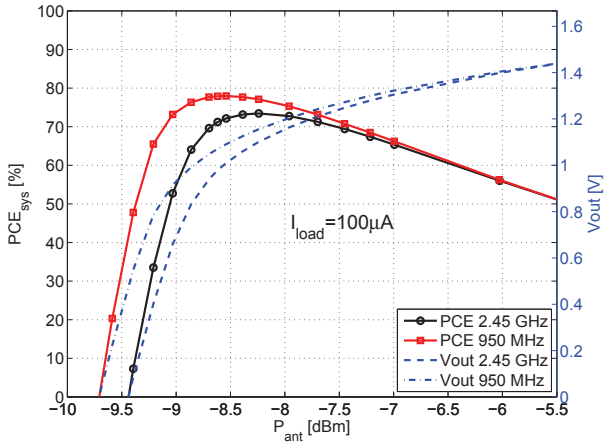

Fig. 8. Simulated system efficiencies at 25 °C of the 2.45 GHz and 950 MHz 2-stage rectifier designs matched with a 50 Ω unit-gain antenna. The antenna input power P_{ant} includes impedance mismatch. The load current is 100 µA.

TABLE II. CHARACTERISTICS AND PEAK PERFORMANCE OF THE SIMULATED MATCHED RECTIFIERS

Frequency	L_m	C_m	P_{ant}	PCE$_{sys}$	V_{out}
MHz	nH	fF	dBm	%	mV
950	48.14	372	-8.54	77.9	1091
2450	18.88	73	-8.24	73.4	1101

PCE$_{sys}$ is defined by (2) where P_{ant} is the available power at the antenna and $P_{in,m}$ is the averaged input power of the matching network. The overall system efficiency has been evaluated in Fig. 8 as a function of antenna received power. The peak performances obtained are reported in table II.

IV. CONCLUSION

The presented automated design methodology for transistor and capacitance sizing of the DD and CC rectifier architectures provides a more systematic design approach to compare architectures than in [7]. The method is applied to design 2-stage CC/DD rectifiers in 65 nm CMOS at 950 MHz and 2.45 GHz with 79.9% and 76.6% PCE, respectively. These have been matched with lumped elements to a unit-gain 50 Ω antenna to assess overall system efficiency. The rectifiers designed at 950 MHz and 2.45 GHz provide 100 µW output power at -8.84 and -8.56 dBm, respectively, resulting in overall power conversion efficiencies of 76.5% and 71.8%. These results are comparable with reports at 100 µW in literature as shown in table III.

TABLE III. RESULTS COMPARED WITH UHF LITERATURE

Passive rectifiers		2009 [6]^b	2013 [8]	**This work**		2013 [9]^c
Improvement		–	Auxiliary stages	optimized CC/DD		Referenced biasing
Frequency	MHz	953	950	950	2450	2400
No. of stages		1	3	2		3
Load		10 kΩ	20 kΩ	100 µA		30 kΩ
Output power	µW	100	100	100		100
Output voltage	V	1	1.41^a	1		1.73^a
VCE	%	–	64.7^a	76.2	75.6	66^a
Input Power	dBm	-7.17^a	-8.38^a	-8.84	-8.56	-8.24^a
PCE	%	52.2^a	69^a	76.5	71.8	66.7
CMOS Tech.	nm	180	130	65		130

a estimated from available data b measurements c post-layout simulations

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