Field-effect memory transistors based on arrays of nanowires of a ferroelectric polymer

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ABSTRACT

Ferroelectric poly(vinylidene fluoride-co-trifluoroethylene), P(VDF-TrFE), is increasingly used in organic non-volatile memory devices, e.g., in ferroelectric field effect transistors (FeFETs). Here, we report on FeFETs integrating nano-imprinted arrays of P(VDF-TrFE) nanowires. Two previously-unreported architectures are tested, the first one consisting of stacked P(VDF-TrFE) nanowires placed over a continuous semiconducting polymer film; the second one consisting of a nanostriped blend layer wherein the semiconducting and ferroelectric components alternate regularly. The devices exhibit significant reversible memory effects, with operating voltages reduced compared to their continuous film equivalent, and with different possible geometries of the channels of free charge carriers accumulating in the semiconductor.

Keywords: FeFETs, ferroelectric polymer, semiconducting polymer, nano-imprint, nanowires, organic memory

1. INTRODUCTION

Ferroelectric poly(vinylidene fluoride-co-trifluoroethylene), P(VDF-TrFE), is attracting renewed interest for use in organic non-volatile memory devices, *e.g.*, in ferroelectric field effect transistors (FeFETs).[1-14] P(VDF-TrFE) crystallizes predominantly in a polar ferroelectric phase characterized by a remnant polarization P_r of *ca.* 60-90 mC/m^2 and a coercive field E_c of *ca.* 50 MV/m. In a FeFET, information is stored in two different permanent polarization states of the ferroelectric film, associated to bits 1 and 0. The direction of the two polarization states can be switched by applying a so-called operation voltage; the reading capability is realized by detecting the source-drain current flowing through a film of a semiconducting material stacked over the ferroelectrics, which is modulated by the permanent polarization state of the ferroelectrics. Organic memory devices like FeFETs have as advantages a non-destructive readout, a good flexibility, a low weight, and easy processing conditions.

However, there is still a strong potential to reduce the operation voltage, to decrease the feature sizes of the device, and to explore new device configurations for both fundamental researches and commercial applications. In this context, we have recently developed nano-imprint lithography (NIL) as a tool to address these points. By NIL, ferroelectric P(VDF-TrFE) is shaped into arrays of nanowires; as a side benefit of this process, preferential crystal orientation occurs, resulting in improved ferroelectric performance. Here, we report on FeFETs integrating such arrays of ferroelectric polymer nanowires. Two different original architectures are tested, the first one consisting of stacked P(VDF-TrFE) nanowires placed over a continuous semiconducting polymer film; the second one consisting of a nanostriped blend layer wherein the semiconducting and ferroelectric components alternate regularly, leading to lateral electrostatic coupling (as opposed to the usual vertical coupling of standard FeFETs).

2. METHOLOGY

2.1 Materials

The ferroelectric P(VDF-TrFE) with 70 molar % of VDF units and a weight-average molar mass of *ca.* 300 000 g/mol (Figure 1) was provided by Solvay Specialty Polymers. The semiconducting poly(triaryl amine) (PTAA, Figure 1) was purchased from Flexink. P(VDF-TrFE) was dissolved in acetylacetone (35 g/L or 60 g/L) and PTAA was dissolved in toluene (5 or 10 g/L). All solutions were filtered by PTFE filters with 0.45 μm pore size before spincoating.

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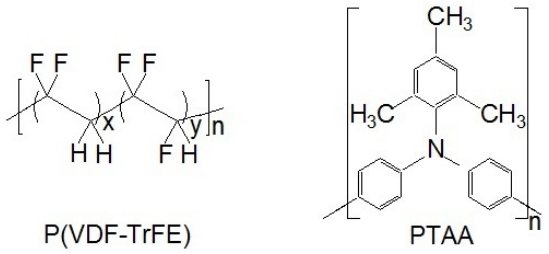

Figure 1. Chemical structures of the ferroelectric polymer P(VDF-TrFE) and the semiconducting polymer PTAA.

2.2 Nano-imprint lithography

Nano-imprint lithography is a high resolution technique which can replicate the nanofeatures of a hard mold by pressing it into a targeted soft film, in order to create nanostructures of virtually any shape. When NIL is applied to (semi)crystalline materials which are capable to self-organize and imprinting conditions are appropriately selected, it may also control their crystallographic orientation and morphology, resulting in the improvement of the functional properties of the materials.[15-20]

In the present work, NIL was employed to shape ferroelectric P(VDF-TrFE) thin films. Figure 2 shows the scheme of the nano-imprint process on a P(VDF-TrFE) thin film (only the cross sections of the mold and sample are drawn). As shown in Figure 2a, a hard mold consisting of line nano-patterns was placed over the spin-coated P(VDF-TrFE) film. The protrusion width *w*, the height *h*, and the spacing *s* between two protrusions are 200 nm. The mold was coated by an anti-adhesion mono-layer. Then the mold was pressed into the film at a pressure of 60 bar and at a temperature of 135 °C (Figure 2b). The selected imprinting temperature was in between the Curie point and the melting point of P(VDF-TrFE) in order to imprint in the liquid crystalline paraelectric phase. The thickness of the P(VDF-TrFE) film was also carefully selected in order to make sure P(VDF-TrFE) crystallizes in a fully confined state (Figure 2b). After 10 min imprinting time, the system was cooled down to room temperature and the mold was removed (Figure 2c), leading to well-defined P(VDF-TrFE) nanowires. Figure 2 (d, e) shows the atomic force microscopy (AFM) topography and phase images of a typical example of fully-confined P(VDF-TrFE) nanowires.

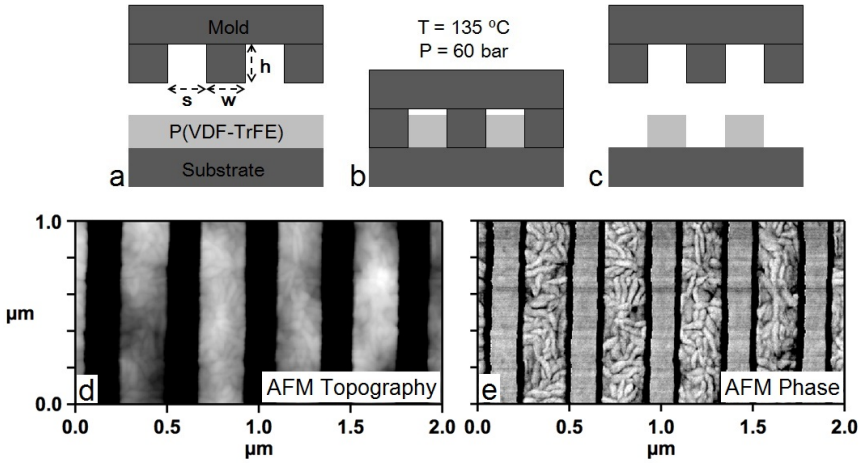

Figure 2. (a, b, c) Scheme of the nano-imprint process on a ferroelectric P(VDF-TrFE) thin film. The mold with line patterns was used in this work. The geometric parameters of the mold are shown in scheme a with $s = w = h = 200$ nm. (d) AFM topography image and (e) AFM phase image of a sample with fully-confined P(VDF-TrFE) nanowires.

It has been proven that crystallographic orientation of P(VDF-TrFE) can be well controlled during imprinting, resulting in a decreased coercive field. This suggests that the operation voltage might be reduced in a memory device employing nano-imprinted P(VDF-TrFE) as information storage medium. In addition, a second functional component can be placed in the openings of the imprinted P(VDF-TrFE) nanowires, and the unique imprinted nano-structures allows us to study the coupling behavior between two functional materials on the nanoscale and to design new device configurations.

Therefore, based on these two beneficial effects from NIL, we have designed FeFETs with two different configurations as sketched in Figure 3: the first one consists of nano-imprinted P(VDF-TrFE) nanowires stacked over a continuous semiconducting PTAA layer (nano-imprinted traditional FeFET) and the second one consists of alternated P(VDF-TrFE) nanowires and PTAA nanowires forming a hybrid layer (hybrid nano-imprinted FeFET). Both FeFETs are discussed in Section 3.

2.2 Device fabrication

Both FeFETs employed a planar substrate with buried source-drain electrodes. First, a Si substrate was treated by thermally-growing a 200 nm SiO_2 layer. Then the patterns of source and drain electrodes were defined by standard photolithography followed by a proper development. After that, a step of local etching of 30 nm SiO_2 was performed before final deposition of 5/25 nm Cr/Au and metal lift-off. These processes led to buried interdigitated source-drain electrodes in an almost perfectly planar substrate. The designed channel length and the channel width are 2 μm and 31 mm, respectively. The electrodes are inter-separated by SiO_2 of 2μm width. The whole transistor covers an area of 500 μm x 500 μm.

In the case of a nano-imprinted traditional FeFET, the PTAA (10 g/L) solution was spin-coated at 2000 rpm for 1 min on the buried source-drain substrate, resulting in the deposition of *ca.* 45 nm PTAA. A 35 g/L P(VDF-TrFE) solution was then spincoated at 3500 rpm for 1 min on the PTAA layer. The P(VDF-TrFE) film, of *ca.* 95 nm initial thickness, was nano-imprinted under the conditions described above with an Obducat imprinter. During imprinting, the line-pattern direction of the mold was placed parallel to the source-to-drain direction. After imprinting, the resulting P(VDF-TrFE) nanowires were of *ca.* 200 nm width, 200 nm spacing , and 185 nm height. They were effectively isolated from each other, since the initial thickness of the P(VDF-TrFE) layer was selected to be *ca.* 95 nm in order to ensure nano-imprinting in full confinement. A mobile conductive AFM tip was used as gate electrode to finalize the device fabrication. The resulting device configuration is shown in Figure 3a. A traditional reference FeFET was also fabricated in order to compare its performance with the nano-imprinted one. For the reference device, a 60 g/L P(VDF-TrFE) solution was spincoated at 3500 rpm for 1 min on the PTAA layer, resulting in a film of thickness equal to the height of the ferroelectric nanowires in the nano-imprinted device. This reference device was annealed at 135 °C for 10 min on a hot plate to improve the crystallinity of the P(VDF-TrFE) film.

In the case of the hybrid nano-imprinted FeFET, the 35 g/L P(VDF-TrFE) solution was spin-coated at 3500 rpm for 1 min on the buried source-drain substrate. The P(VDF-TrFE) film, of *ca.* 98 nm initial thickness, was nano-imprinted with an Obducat imprinter under the conditions described above. During imprinting, the line-pattern direction of the mold was placed parallel to the source-to-drain direction. The initial thickness of the P(VDF-TrFE) layer was selected to be *ca.* 98 nm in order to ensure nano-imprinting in full confinement. This results in the formation of effectively isolated P(VDF-TrFE) nanowires of *ca.* 200 nm width, 200 nm spacing and 200 nm height, and fully open trenches separating P(VDF-TrFE) nanowires. The PTAA solution (5 g/L) was spin-coated at 2000 rpm for 1 min on the nano-imprinted P(VDF-TrFE) layer, resulting in the deposition of *ca.* 100 nm PTAA between the ferroelectric nanowires and of *ca.* 15 nm PTAA atop of them. A mobile conductive (AFM) tip was used as gate electrode to finalize the device fabrication. Figure 3b shows the idealized configurations of the resulting devices (the ultra-thin PTAA layer atop P(VDF-TrFE) nanowires is not shown here).

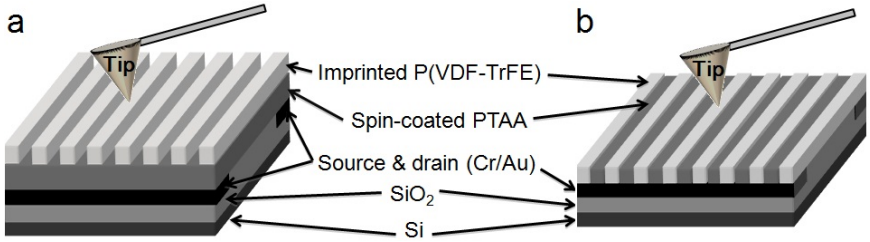

Figure 3. Idealized structures of two field-effect transistors consisting of P(VDF-TrFE) nanowires (a) stacked over a continuous PTAA layer and (b) alternated with PTAA nanowires, forming a hybrid layer. Both FeFETs use a mobile conductive atomic force microscopy tip as gate electrode.

2.3 Device characterization

The thickness of the PTAA layer and of the P(VDF-TrFE) layer was characterized by AFM in tapping mode with a silicon cantilever (PPP-NCHR from Nanosensors): layers at different stages of the fabrication process were scratched down to the SiO_2 layer, and the topography of the sample was measured taking the bottom of the scratch as reference for height.

Piezoresponse force microscopy (PFM) in contact mode was used to characterized the piezoresponse of the ferroelectric P(VDF-TrFE) layer/nanowires. Figure 4 shows a typical example of PFM amplitude image and phase image obtained with a 100 nm-thick continuous P(VDF-TrFE) thin film sample. A strong contrast appears in both images between poled and unpoled regions, indicating that the dipoles are aligned along the direction of the poling field. The direction of dipole moments or polarization of P(VDF-TrFE) on different regions is shown in Figure 3c. In this work, an Agilent 5500 AFM (Agilent Technologies) system equipped with a Mac III Controller lock-in amplifier was adapted to the requirements of the PFM technology. The source-drain electrodes were used as bottom electrodes. A conductive Si cantilever (Boron-doped diamond-coated, CDT-CONTR from Nanosensors) was used as a scanning top electrode. The piezo/ferro-electric response was characterized in PFM imaging mode with an oscillating ac voltage of 0.5 V amplitude and no added dc bias. All PFM measurements were made by applying the ac driving bias V_{tip} on the tip, while the poling was done by applying a dc bias $V_{s\&d}$ on the source-drain electrodes while scanning the grounded tip. Here, we define the poling voltage $V_{pol} = V_{tip} - V_{s\&d} = -V_{s\&d}$.

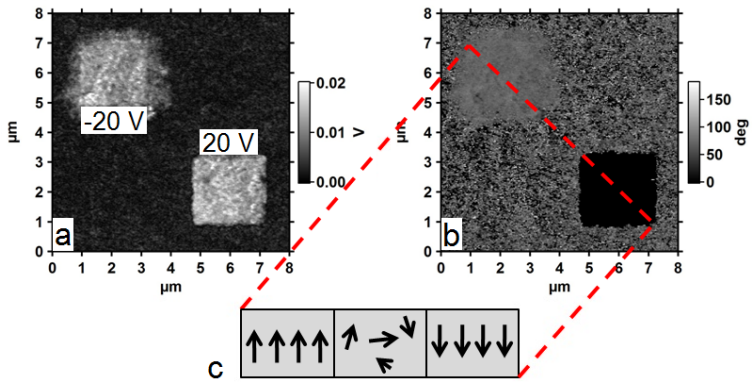

Figure 4. PFM (a) amplitude and (b) phase images of a 100 nm-thick P(VDF-TrFE) film deposited on a conductive doped Si substrate. The direction of dipole moments or polarization on different regions is shown in panel c.

The current characterization of the device was performed with a Keithley analyzer (Model 6430). The source-drain current I_{ds} was measured upon removal of the poling gate voltage at a fixed value of source-drain voltage V_{ds}.

3. RESULTS AND DISSCUSSIONS

3.1 Nano-imprinted traditional FeFET

The operation voltage of a FeFET intrinsically depends on the switching behavior of P(VDF-TrFE) dipoles or polarization. Easier switching results in a lower operation voltage. Therefore, the switching behavior of the continuous and nano-imprinted P(VDF-TrFE) films in a traditional FeFET configuration was firstly studied by PFM as shown in Figure 5. For both films, the piezoresponse contrast changes depending on the previously-applied poling voltage $V_{s\&d}$: 10 V bias is not sufficient to align the P(VDF-TrFE) dipoles and to result in a PFM contrast; starting from 15 V for the continuous film and 12.5 V for the nano-imprinted film, the PFM contrast starts to appear due to partial alignment of the P(VDF-TrFE) dipoles. The contrast increases when increasing $V_{s\&d}$ and reaches a maximum when $V_{s\&d}$ is large enough to permanently align most dipoles in one direction. The maximum contrast means that the saturation polarization P_r is obtained. To determine at which voltage the maximum P_r can be obtained, the normalized phase contrast was plotted versus $V_{s\&d}$ in Figure 5e for both the continuous and nano-imprinted P(VDF-TrFE) films. Here, the phase contrast was defined as $A_0\cos\varphi_0 - A\cos\varphi$ and normalized to have similar saturation P_r, where A_0 and φ_0 are the average amplitude and the average phase of the background; A and φ are the average amplitude and phase of the smaller square areas where $V_{s\&d}$ was applied. As shown in Figure 5e, the contrast reaches a maximum at 20 V and a plateau is obtained for $V_{s\&d}$ larger

than 20 V for the nano-imprinted P(VDF-TrFE) film, while this point is 27.5 V for the continuous P(VDF-TrFE) film. This means that the switching field of the nano-imprinted P(VDF-TrFE) is indeed lower than the one of the continuous film, given the fact that the thickness of the continuous film was equivalent to the height of the nanowires of the nano-imprinted sample. For instance, at 15 V, *ca.* 5% of the maximum polarization contrast is obtained for the continuous film, whereas *ca.* 60% is obtained for the nano-imprinted film. Hence, the P(VDF-TrFE) dipoles are more easily aligned in nanowires than in the continuous film, with a switching voltage reduced by a factor of about 1.5.

Then, the current characterization of the FeFETs was performed. A conductive AFM tip was used as a grounded gate which was scanned over a defined area of 50 µm x 50 µm while setting $V_{s\&d}$ to a given value, in order to pole the system at $V_{pol} = -V_{s\&d}$. Then, after removal of the tip, the polarization-induced source-drain current I_{pol} was measured by applying a source-drain voltage V_{ds} of 10 V. Here, I_{pol} is defined as $I_{pol} = I_{ds} - I_{initial}$, where $I_{initial}$ is the source-drain current I_{ds} measured after scanning at $V_{pol} = 0$ V. This definition of the polarization-induced current rests on the fact that P(VDF-TrFE) cannot be polarized at 0 V poling voltage, resulting in $I_{pol} = 0$. For both the reference and the nano-imprinted FeFET, I_{pol} is plotted in Figure 6 versus the previously-applied V_{pol} at $V_{ds} = 10$ V.

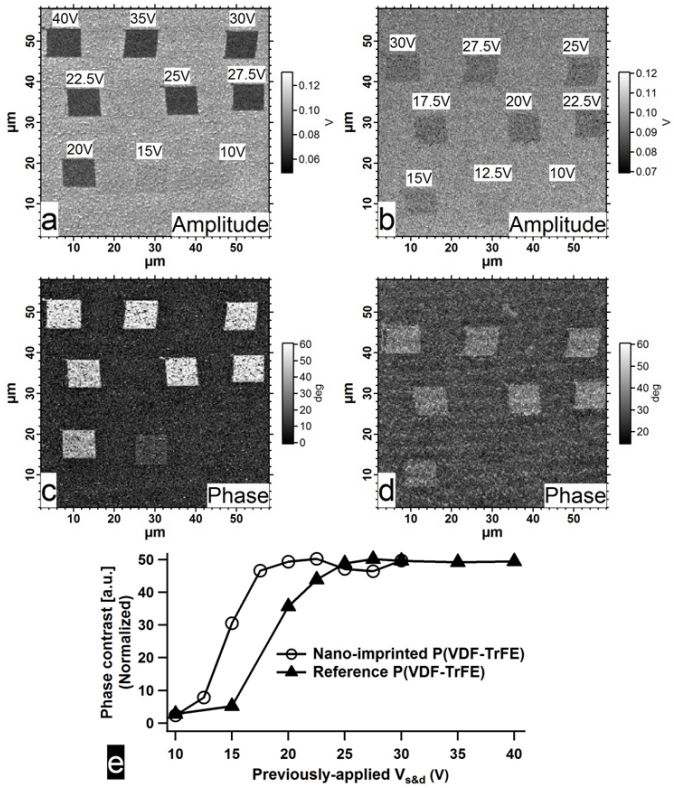

Figure 5. PFM (a) amplitude and (c) phase images for the continuous P(VDF-TrFE) in a reference FeFET; PFM (b) amplitude and (d) phase images for the nano-imprinted P(VDF-TrFE) in a nano-imprinted FeFET. In all images the background was polarized initially with a dc voltage of 0 V, and the smaller areas of 8 µm x 8 µm were polarized with increasing positive dc voltages $V_{s\&d}$ applied on source-drain electrodes (values given in panels a and b). All PFM images were recorded with a 0 V dc voltage; PFM piezoresponse phase contrast versus source-drain voltage $V_{s\&d}$ for (e) the continuous P(VDF-TrFE) and (f) for the nano-imprinted P(VDF-TrFE).

Figure 6 presents the transfer characteristics with a clear hysteresis for both the reference and the nano-imprinted FeFETs. I_{pol} saturates below $V_{pol} = -30$ V and -20 V for the reference and nano-imprinted FeFET, respectively. This means that the operation voltage (to write a data '1') is decreased by a factor of *ca.* 1.5 in the imprinted FeFET ($V_{NIL,1}$) compared to the reference FeFET ($V_{ref,1}$). This is a significant improvement for the performance of the FeFET memory. When sweeping back V_{pol}, I_{pol} goes back close to its initial value above 25 V and 20 V for the reference and nano-imprinted FeFETs, respectively. This again confirms that, to write a '0', the operation voltage $V_{NIL,0}$ for a nano-imprinted FeFET is reduced compared to a reference FeFET ($V_{ref,0}$).

Note that the saturation value of I_{pol} for the reference FeFET is *ca.* 2.5 times larger than that of the nano-imprinted FeFET. This is because the fill factor of the mold is 0.5 and some defects were created during the imprinting, resulting in the active area of the nano-imprinted FeFET being less than half of that of the reference FeFET. This suggests that each P(VDF-TrFE) nanowire acts more or less in isolation from its neighbors, and the nano-imprinted transistor actually consists of a series of nanowire transistors placed in parallel. Hence, the system is potentially suitable for a strong reduction of memory size, possibly down to one single nanowire.

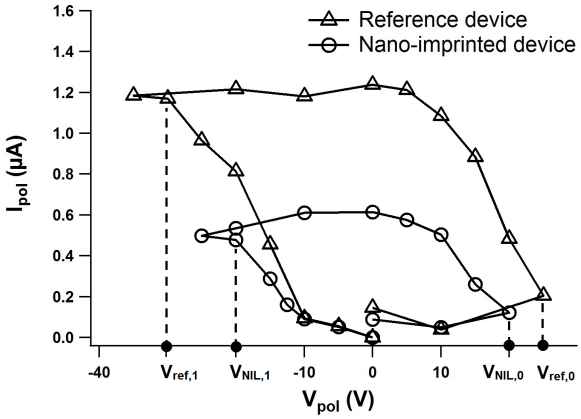

Figure 6. Transfer characteristics of a reference and a nano-imprinted FeFET. The polarization-induced current I_{pol} was measured at V_{ds} = 10 V upon removal of V_{pol}. The tip electrode scanning size for both FeFETs was 50 µm x 50 µm. Because the fill factor of the mold is 0.5, the equivalent active area is 25 µm x 25 µm for the nano-imprinted FeFET. The measurement was started at V_{pol} = 0 V, performed with a clockwise sequence, and finished again at V_{pol} = 0 V. The operation voltages to write the data '1' and '0' for the reference FeFET ($V_{ref,1}$, $V_{ref,0}$) and the nano-imprinted FeFET ($V_{NIL,1}$, $V_{NIL,0}$) are indicated in the graph.

3.2 Hybrid nano-imprinted FeFET

Since the nature of the substrate (Au regions or SiO_2 regions, indicated by green dashed lines in Figure 7a) lying below the ferroelectric nanowires is not the same, different switching and stabilization behaviors of the polarization might appear. PFM was again used to study the switching behavior of the ferroelectric nanowires in the hybrid layer. Two defined regions (8 µm x 8 µm for each) were first poled by scanning the grounded tip while applying a 20 V or -20 V dc voltage simultaneously to the source and drain electrodes ($V_{s\&d}$). The sample was then imaged in PFM mode at zero dc bias (25 µm x 25 µm).

In the case of poling the system at $V_{s\&d}$ = -20 V (the left-top boxed regions of Figure 7), a strong contrast is observed in both PFM amplitude and phase images for P(VDF-TrFE) nanowires lying over the Au regions, compared to regions that were not poled; however, no contrast appears for poled P(VDF-TrFE) nanowires lying over the SiO_2 regions. This indicates that, upon removal of the poling voltage, the P(VDF-TrFE) dipoles remain aligned when lying over the conducting Au electrodes and are in a randomly-oriented state when lying over the insulating SiO_2 regions. In the case of poling the system at $V_{s\&d}$ = 20 V (the right-bottom boxed regions of Figure 7), a strong contrast compared to regions that were not poled can now be observed in PFM phase and amplitude for P(VDF-TrFE) irrespective of its location over Au electrodes or SiO_2 regions. This indicates that the P(VDF-TrFE) dipoles are aligned over the full poled area after removal of the poling voltage, even when P(VDF-TrFE) nanowires rest over insulating SiO_2 regions.

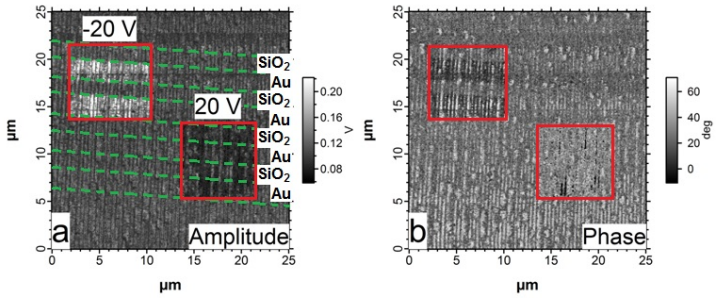

Figure 7. PFM piezoresponse of a hybrid P(VDF-TrFE)/PTAA nano-striped layer. (a) amplitude image, and (b) phase image of the same region of the transistor. The Au electrodes and interspersing SiO_2 regions lying below the hybrid layer are indicated in panel a by green dashed lines. In both images smaller square regions of 8 µm x 8 µm (red-boxed in the images) were polarized by scanning the grounded tip while applying a 20 V or -20 V dc voltage on source and drain electrodes ($V_{s\&d}$, indicated in panel a). Then PFM images of 25 µm x 25 µm area were subsequently recorded with a 0 V applied dc voltage.

When a ferroelectric material is poled by a sufficient electric field, its dipoles align along the direction of the field, resulting in surface charges accumulating at the ferroelectric interface. However, when the poling field is removed, the accumulated surface charges must be screened or effectively reduced to decrease the polarization energy.[21] As a consequence, in order for a ferroelectric material to be stable after poling, compensating charges must be provided at its interface to suppress the depolarizing field resulting from its polarization. In our system, when P(VDF-TrFE) nanowires are poled over bottom Au electrodes, compensating charges are provided at the bottom interface by the free carriers of Au (electrons or holes, depending on the sign of the ferroelectric polarization). As for the top interface, compensating charges are probably charged active ions from the thin water layer present in air on the top free surface. Therefore, the P(VDF-TrFE) dipoles remain aligned atop the Au electrodes upon removal of positive or negative poling voltages, resulting in two stable polarization states of P(VDF-TrFE) over Au electrodes.

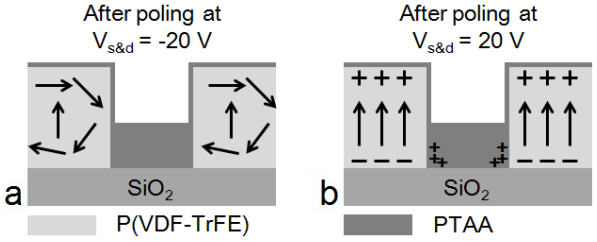

Figure 8. Sketch of the polarization states of P(VDF-TrFE) nanowires lying atop SiO_2. (a) randomly-oriented polarization state after downward-poling (V_{tip} = 0, $V_{s\&d}$ = -20 V). (b) Laterally-screened polarized state after upward-poling (V_{tip} = 0, $V_{s\&d}$ = 20 V). Arrows indicate the idealized direction of the dipoles and the ferroelectric polarization of P(VDF-TrFE) nanowires (possible horizontal components of the polarization are not shown in this idealized cartoon); the lateral accumulation of holes in the PTAA is also shown in panel b.

However, the switching and stabilization behaviors are different for P(VDF-TrFE) dipoles resting atop insulating SiO_2. Compensating charges are still provided at the top interface by the same mechanism as in the case of Au electrodes. But at the bottom interface, no compensating charges can be provided by the insulating SiO_2. Therefore, P(VDF-TrFE) dipoles should be in a randomly-oriented state and no PFM contrast should appear upon removal of the poling field, which is indeed the case when $V_{s\&d}$ = -20 V as shown in Figure 7 and Figure 8a. In contrast, for $V_{s\&d}$ = 20 V, the PFM contrast unexpectedly appears in both amplitude and phase images as shown in Figure 7, which indicates P(VDF-TrFE) dipoles aligned upwards by the field are stabilized. This switching and stabilization behavior can only be due to the p-type PTAA lying on the lateral side of P(VDF-TrFE) nanowires. In PTAA, positive holes are injected and accumulate at the P(VDF-TrFE)/PTAA/SiO_2 interface as drawn schematically in Figure 8b, which results in a stable P(VDF-TrFE) polarization state upon removal of the poling voltage. This switching and stabilization mechanism cannot be operative for the opposite poling voltage, since it would then require the injection and accumulation of negative charges, *e.g.* electrons, at the P(VDF-TrFE)/PTAA/SiO_2 interface, which is not possible due to the p-type nature of PTAA. We should note that the switching and the stabilization behaviors of the ferroelectric polarization might be more complex than described above. In this context it is worth pointing out that, even for classical FeFETs, a complete understanding/

explanation of the switching and stabilization mechanism remains so far elusive.[8, 13, 22-25] Therefore, future work needs to be done in order to get a complete illustration of the switching and stabilization mechanism.

Although the exact switching and stabilization mechanism of P(VDF-TrFE) polarization remains elusive, the effect of lateral charge screening in the absence of direct contact with an underlying metal electrode already provides the possibility to fabricate memory devices with new configurations. As shown in Figure 3b, we now demonstrate the memory functionality of a hybrid nano-imprinted FeFET. Here, we again used the PFM conductive tip as the mobile gate of the transistor to pole the P(VDF-TrFE). The grounded tip was scanned over a defined standard area of 50 µm x 50 µm while setting $V_{s\&d}$ to a given value, in order to pole the system at V_{pol} (again defined as $V_{pol} = V_{tip} - V_{s\&d} = -V_{s\&d}$). Then, the poling tip was removed and the polarization-induced current I_{pol} was measured at a source-drain voltage V_{ds} of 10 V. I_{pol} is again defined as $I_{pol} = I_{ds} - I_{initial}$, where $I_{initial}$ is the source-drain current I_{ds} measured after the scanning at $V_{pol} = 0$ V. $I_{initial}$ is also equivalent to the off current I_{off} of the memory transistor. The current measurement was performed over the complete transistor area of 500 µm x 500 µm, of which only one part of *ca.* 1/100th had been previously polarized by the tip (due to limitations in the scanning range of our PFM setup). Figure 9a shows the polarization-induced current I_{pol} versus the previously-applied poling voltage V_{pol}. When starting from 0 V and the previously-applied poling voltage V_{pol} is larger than -10 V, I_{pol} is close to 0 because the P(VDF-TrFE) is not polarized by an insufficient poling field and no electrostatic coupling between P(VDF-TrFE) and PTAA occurs. This state can be considered as the 'off' state of the memory transistor. I_{pol} then increases for V_{pol} = -12.5 V and reaches a maximum (*ca.* 0.27 µA) when V_{pol} = -20 V, because of the progressive polarization of P(VDF-TrFE) from -12.5 V on, with the maximum polarization being achieved at -20 V. At this stage, mobile holes have accumulated at the P(VDF-TrFE)/PTAA/SiO_2 interface as shown in Figure 8b, creating a conducting channel which results in a higher current. This state can be considered as the 'on' state. After reaching the maximum value, I_{pol} keeps almost constant when the previously-applied poling voltage V_{pol} is progressively increased to 5 V. This is due to the accumulation of the holes at the P(VDF-TrFE)/PTAA/SiO_2 induced by the stable polarization of the P(VDF-TrFE) nanowires. From 10 V on, I_{pol} starts to decrease and comes back to its initial 0 state for V_{pol} = 20 V. This is because the polarization direction of P(VDF-TrFE) starts to be changed from 10 V on, with the polarization being switched into opposite or random directions depending on the P(VDF-TrFE) location (atop Au or SiO_2) for V_{pol} = 20 V. At this stage, no mobile charges accumulate at the P(VDF-TrFE)/PTAA/SiO_2 interface, resulting in almost 0 I_{pol} values. These operations form a clear current hysteresis and two current states can be obtained, which can be used to store data 1 and 0 for memory applications.

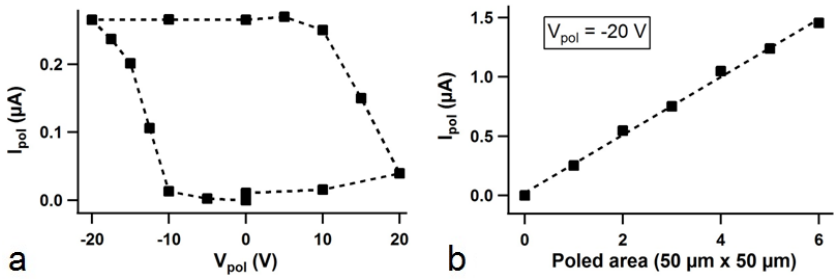

Figure 9. Current characterization of the hybrid FeFET. (a) Polarization-induced current I_{pol} (measured after poling one standard area 50 µm x 50 µm at V_{pol}, followed by removal of V_{pol} and application of V_{ds} = 10 V) versus previously-applied poling voltage V_{pol}. (b) Polarization-induced current I_{pol} (measured upon removal of V_{pol} = -20 V) versus the total poled area. The total poled area is expressed as the number of standard poling areas of 50 µm x 50 µm size, each standard area corresponding to a different poling scan in the AFM.

As mentioned before, the poling area is only 50 µm x 50 µm due to the limitation of our PFM setup, whereas the current characterization was performed over the complete transistor area of 500 µm x 500 µm. Therefore, the active area is only 1/100th of the complete transistor area. This is the reason why the measured I_{pol} is limited (*ca.* 0.27 µA). Therefore, we have poled several regions of 50 µm x 50 µm in order to obtain a larger active area and to check the influence of the previously-poled area over the polarization-induced current. Figure 9b shows that I_{pol} increases linearly with the poled area. This actually provides the possibility to store more than two values in the memory device, by poling the hybrid layer over different defined standard areas. In Figure 9b for instance, seven different values could be stored in the device. This also indicates that P(VDF-TrFE)/PTAA nanowires work independently, which again suggests that the size of the memory device can be well reduced possibly down to one single P(VDF-TrFE)/PTAA nanowire.

3.3 Comparison of memory FeFETs with different configurations

To have a better view of memory FeFETs with different configurations and to guide efforts which should be taken in the future for further improvement, the advantages and disadvantages of the nano-imprinted FeFETs reported above are summarized in Table 1 and compared to a reference FeFET with a continuous P(VDF-TrFE) storage layer. Nano-imprinted FeFETs have as advantages a low operation voltage and a potential to scale down the memory size. In addition, the lateral screening effect of polarization charges, which is a new discovered effect, offers opportunities to design other configurations, and could be exploited further. Nevertheless, much more work is required in order to optimize the fabrication process and to increase the performances of nano-imprinted FeFETs.

Table 1. Comparison of memory FeFETs with different configurations

	Advantages	Disadvantages
Reference FeFET	Easy fabrication of fully functional devices Good stability Acceptable on/off ratio	High operation voltage Large memory size
Nano-imprinted traditional FeFET	Lower operation voltage Potential to scale down to one single nanowire transistor Acceptable on/off ratio	Isolation between the semiconductor and the gate needed for full integration Stability needs to be checked
Hybrid nano-imprinted FeFET	Lower operation voltage Potential to scale down to one single nanowire transistor Newly-reported lateral screening of polarization charges widening the design of new memory device architecture	Isolation between the semiconductor and the gate needed Stability needs to be checked On/off ratio needs to be improved

4. CONCLUSIONS

To summarize, we have developed NIL to shape ferroelectric P(VDF-TrFE) thin films. Based on NIL, we have designed two kinds of FeFETs, a traditional FeFET with nano-imprinted ferroelectric layer, and a hybrid nano-imprinted FeFET, and integrated this technology in the fabrication process of these two FeFETs.

In the case of a nano-imprinted traditional FeFET, P(VDF-TrFE) nanowires on top of PTAA showed a decreased switching field compared to a continuous film. In addition, the electric field needed to maximize the remnant polarization P_r was significantly decreased by a factor of *ca.* 1.5 compared to a continuous film. The current characterization showed that a smaller poling voltage was needed to reach the maximum polarization-induced current for the nano-imprinted FeFET compared to the homogeneous reference. This leads to a decreased operating voltage for the memory application.

In the case of a hybrid nano-imprinted FeFET, we have developed a nanostriped organic hybrid layer by shaping ferroelectric P(VDF-TrFE) into nanowires, followed by filling the openings by PTAA. This process leads to the easy creation of well-controlled hybrid nanostructures over a buried source-drain electrode substrate. In this system, when a poling field with the proper polarity is applied, the ferroelectric dipoles of P(VDF-TrFE) nanowires can be stabilized by charges accumulating laterally in the PTAA nanowires even when the P(VDF-TRFE) nanowires rest over the insulating SiO_2. This lateral accumulation of mobile charges in PTAA provides the possibility to fabricate a new memory device, based on the intrinsic storing/reading capability of the hybrid nanowire layer. The current characteristics of the memory device showed a current hysteresis as typically obtained in a traditional FeFET. We also showed that the current could be scaled by changing the poled area of the device, thereby providing the possibility to store more than two states in one single transistor.

For both FeFETs, we have showed that the ferroelectric nanowires work independently. Therefore, our methodology to fabricate FeFETs consisting of ferroelectric nanowires offers interesting possibilities for a strong size reduction of organic memory devices. However, further technical work is required to fabricate fully functional devices.

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