Compact modeling of the high temperature effect on the single event transient current generated by heavy ions in SOI 6T-SRAM

E. Boufouss, J. Alvarado and D. Flandre
Université catholique de Louvain (UCL)
Microelectronics laboratory (Institute ICTEAM)
Bâtiment Maxwell, Place du Levant, 3
B-1348 Louvain la Neuve, Belgium
Email: elhafed.boufouss@uclouvain.be

Abstract

A temperature dependence analysis of the single event transient current induced by heavy ions irradiation is performed in the range of 300K to 500K on a 1µm SOI CMOS MOSFET standard 6T-SRAM cell. The Sentaurus TCAD mixed-mode numerical simulation showed a significant impact of the temperature on the current induced by the radiation and as a result, an increase of the 6T-SRAM sensitivity upon radiation.
A SOI MOSFET compact model introduced in SPICE as a Verilog-A module reproducing the single event effects was developed. This model shows a very good agreement with the TCAD simulations results but with a drastic reduction of the simulation time. Furthermore this model could be extended to other circuits simulations. This result is of importance to allow for extensive circuit design studies which cannot be carried out with TCAD physical simulations.

Key words: Temperature dependence, Heavy ion irradiation, Single event transient, linear energy transfer threshold (LETth), Circuit and device simulation, 6T-SRAM

I. Introduction

Many devices can be exposed to extremely harsh environments as under radiation and at high temperatures, in space applications for example. SOI (Silicon-on-Insulator) circuits are often used thanks to their extended range of working temperature and lower sensitivity to radiation effects [l-3]. Many papers discussed SRAM sensitivity [4-6] and studied their temperature dependence up to 418K [7].
This work presents an extended temperature analysis from 300K up to 500K, under heavy ions radiation for high-temperature SOI circuits. Two different methods were used. The first uses 2-D TCAD (Technology computer aided design) mixed-mode simulations [8-9] to investigate: firstly the current induced in a single SOI MOSFET by the heavy ions particles; secondly the 6T-SRAM sensitivity to radiation at different temperatures, through its linear energy transfer threshold (LET_th). The LET_th is the lowest energy able to create a single event upset SEU, here in the standard 6T-SRAM [10].
The second method uses a dedicated SOI MOSFET compact model introduced in SPICE as a Verilog-A module. The LET_th of the 6T_SRAM is simulated versus temperature. A comparison between both methods shows a good agreement at different temperatures, but with a huge reduction of simulation time and less complicated simulation steps in the second method.

II. Two Dimensional TCAD Simulations

The Sentaurus TCAD simulator is used to simulate the radiation effects, first on a single SOI NMOS transistor and next, on a SOI 6T-SRAM cell.

II.1- Simulation of a Single SOI NMOS Transistor:

We consider a PD (Partially-Depleted) SOI CMOS process featuring 25nm thick gate oxide, 250nm thick silicon body and 1µm thick buried oxide with 1µm channel length, as is typical for present high-temperature applications. Fig1 shows the 2D device structure generated for a SOI MOSFET [11]. Fig.2 (a,b,c) show a fair agreement between the experimental and TCAD drain current (Id) - drain voltage (V_{DS}) curves in off state (gate voltage V_{GS} = 0) for temperatures of 300, 400 and 500K .

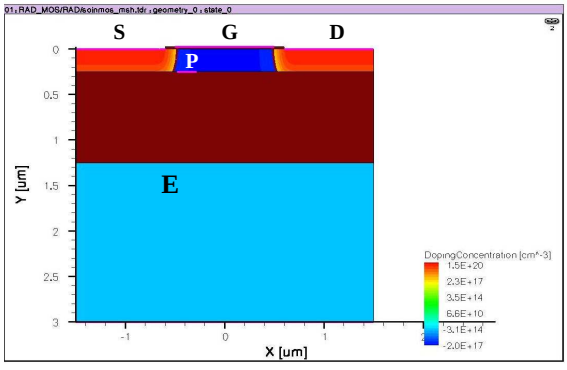

Fig.1 : 2D structure of PD SOI N-MOSFET

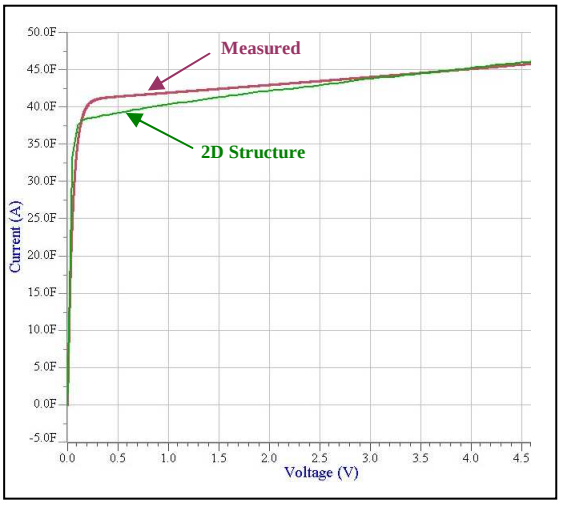

Fig.2a: Drain current versus V_{DS} (V_{GS}=0) at 300K

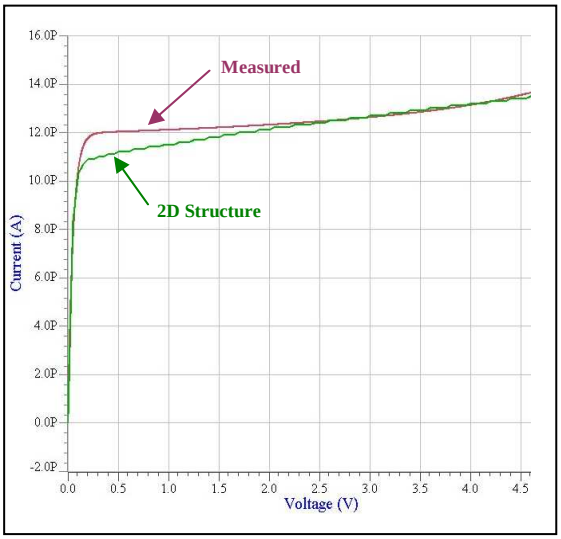

Fig.2b: Drain current versus V_{DS} (V_{GS}=0) at 400K

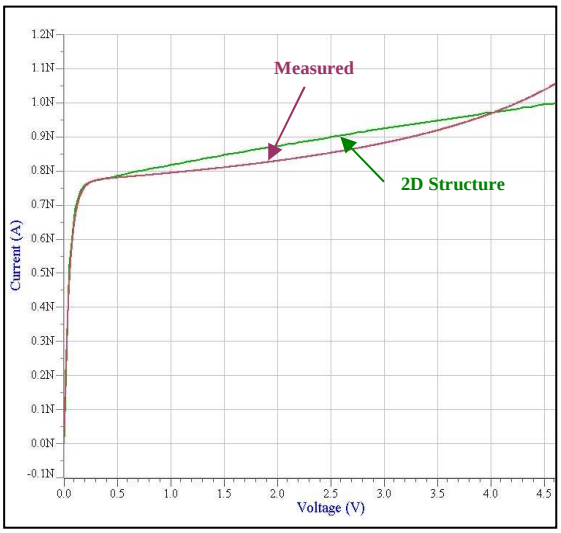

Fig.2c: Drain current versus V_{DS} (V_{GS}=0) at 500K

The OFF state with V_{GS} = 0 and V_{DS} = 4V and a radiation hit on the drain region has been determined as the worst case to study the radiation effect. A heavy ions particle is used with a radius of 0.1 um, an energy of LET=30MeV.cm^2/mg = 0.3pC/µm and a normal incidence (Fig.3).

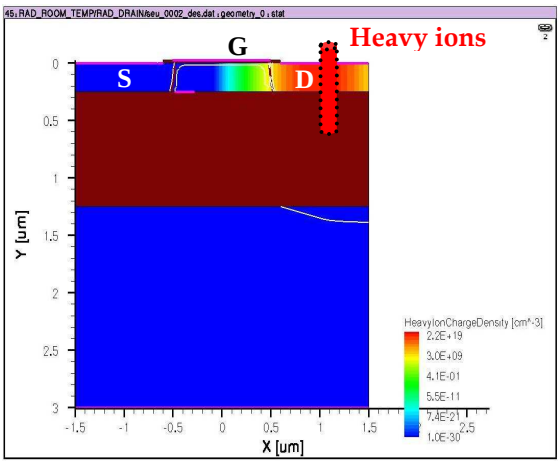

Fig.3 Simulated heavy ion hit in the drain with a normal incidence

The 2-D TCAD simulations allow for extracting the radiation induced current at different temperatures. Fig4 shows the drain current transient after the particles hit for the range of temperatures from 300 to 500K.

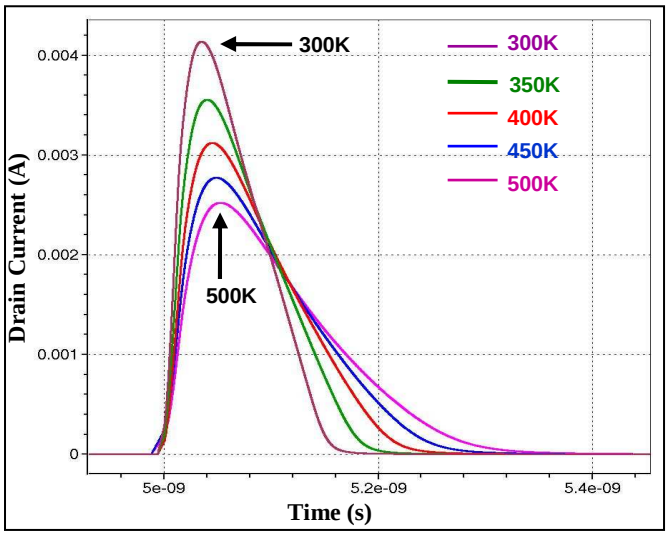

Fig.4: Drain current versus time from 300 to 500K with LET=0.3pC/ µm

As showed in Fig.5, the current pulse amplitude decreases when the temperature increases. The time delay of the current pulse defined at 10% of the maximum is however increased with temperature. Similar results have been found in previous works for a temperature up to 418K [7], [12].

This behavior can be explained for the maximum current amplitude I, by the average of the electron mobility µ [13]:

$$I = < \mu * E_{Field} > LET$$

where E_{Field} is the electric field and LET the energy of the ionized particles. As the mobility µ decreases

with temperature (following $\mu \propto T^{-\alpha}$ with $\alpha > 1.3$), the current pulse amplitude also decreases with temperature.

The delay could be related to the diffusion current, which depends on the diffusion coefficient. The later is related to temperature T and mobility μ by the Einstein relationship [14]:

$$D = \frac{\mu kT}{q} \propto T^{\alpha-1} \quad (1)$$

where q is the electron charge and k the Boltzmann constant.

Equation (1) is not sufficient to explain the simulated linear variation of delay as a function of temperature. This could then be explained by the SOI internal parasitic bipolar effect in which the time constant for the return to equilibrium following an on-to-off transient depends on the bipolar gain β. The later indeed increases linearly with temperature. This hypothesis will be verified in a future work.

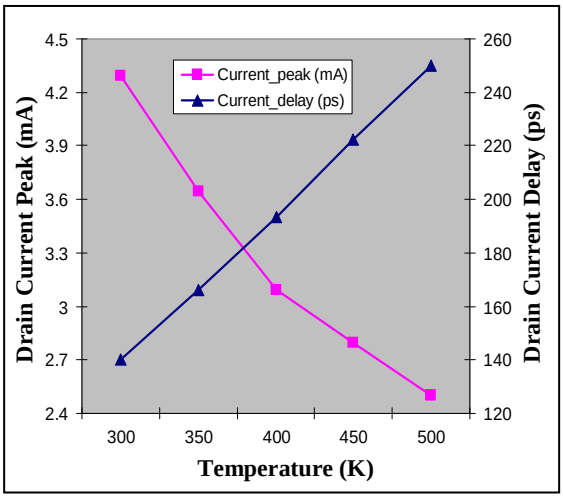

Fig.5 Drain current amplitude and delay time versus temperature for a LET=0.3pC/ μm

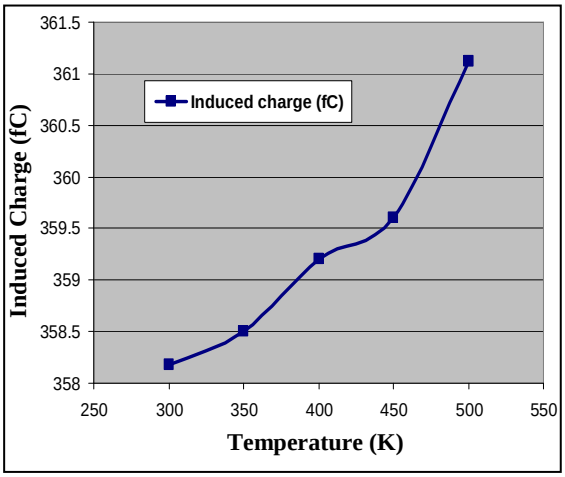

Fig.6 Drain induced charge versus temperature for a LET=0.3pC/ μm

Fig.6 shows a slight increase of the charge induced in the SOI transistor (i.e. the integral of fig. 4 curves) with the temperature, even if the particles LET remains unchanged (0.3pC/μm). In the range of 400 and 450K we note that the slope of the charge increase is reduced.

II.2- Simulation of the SOI CMOS Standard 6T-SRAM cell:

The simulated SOI CMOS 6-T SRAM cell (Fig.7) has 6μm and 12μm channel widths for NMOS and PMOS transistors respectively, both with 1μm channel length. Simulations are performed in memory state (no write, no read). The bit and word lines are pre-charged to VSS (0V). The supply voltage VDD is 4V.

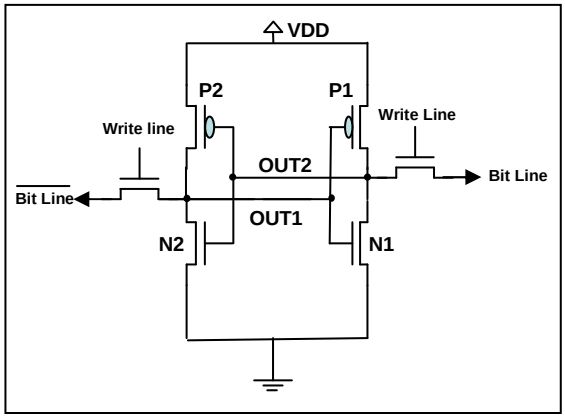

Fig.7 Standard 6T-SRAM cell

As the structure of 6T-SRAM is symmetric and the N-MOSFET is more sensitive to radiation effect than the PMOS [15], the worst case corresponds to a hit on one NMOS transistor in off state (N1 in Fig.7 for example) and is sufficient to evaluate the impact of radiation on the 6T SRAM cell.

We first use the following mixed-mode simulation methodology [16-17]. The principle is to limit the use of the device simulator to the struck NMOS transistor while the rest of the memory cell is represented by SPICE elements (Fig.8).

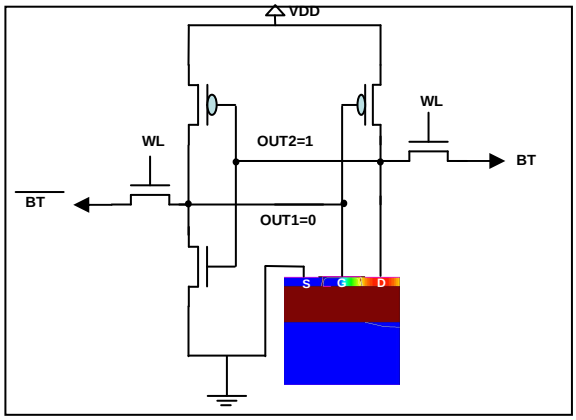

Fig.8 6T-SRAM cell with the 2D structure of the irradiated transistor

Parasitic capacitances extracted from the 6T-SRAM cell layout were included in the mixed-mode netlist to evaluate the right LET_th. Fig.9 shows the simulated LET_th for the 6T_SRAM cell.

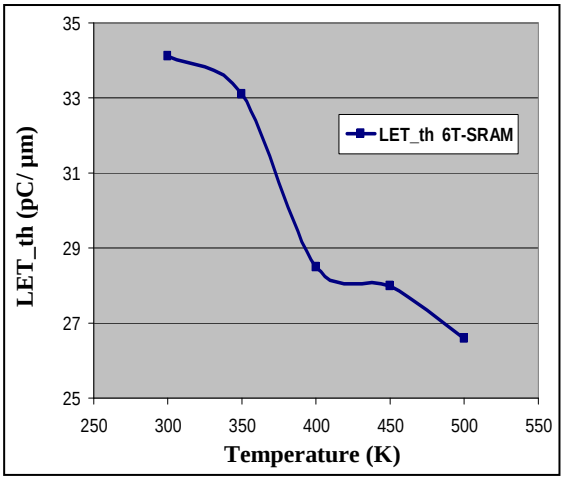

Fig.9 Mixed-mode simulation of the threshold LET for the SOI CMOS 6T-SRAM cell versus temperature

The increase of the temperature decreases the LETth and as a result, it increases the SEU sensitivity of the 6T-SRAM. This sensibility can be explained in part, as in a previous work [7] by the decrease of the threshold voltage V_{th} with temperature increase and in another part, by the increase of the collected charge as discussed above. The LET_th indeed shows the same slope reduction as the charge in the range from 400 to 450K.

III. Compact Model Simulations

Besides the creation and the check of the 2D structure, the TCAD simulation consumes a great time for one simulation; i.e. about two hours for 10ns of transient simulation of the 6T-SRAM, on a workstation with 1.6GHz clock frequency and a 4 GB RAM. In case of 3-D TCAD simulations, several days are needed. Furthermore numerous simulations are needed to find the right LET_th at different temperatures. Due to this complicated approach it is essential to develop a simple model of the single event upset (SEU) which can be simulated directly with SPICE. Many works to model the SEU in Spice are presented in the literature. These works are based on the introduction of a current source between drain and source to model the radiation induced current in the transistor [5] ,[18-19].

The compact model developed in this work is based on the concept of connecting a current source I_{SEU} controlled by voltages, between the body contact and source terminals of the BSIMSOI model. The current source I_{SEU} is defined by the equations of the generation of electron-hole pairs by a heavy ion strike through the channel, used in [21] as:

$$I_{SEU}=\pi\cdot r^2\cdot(J_n+J_p)=\pi\cdot r^2\cdot q\cdot \left[D_n\nabla\rho_n(r,y,t)+\mu_n nE-D_p\nabla\rho_p(r,y,t)+\mu_p(N_A+n)E\right]$$

where J_n and J_p are the electrons and holes current densities, D_n and D_p the diffusion coefficients of electrons and holes, μ_n and μ_p the mobilities of electrons and holes, n the electron-hole pair concentration generated by the ion track, N_A the doping concentration, $\nabla\rho_n$ and $\nabla\rho_p$ the gradients of electrons and holes generated by the ion track.

The injected current in the body I_{SEU} constitutes the base current of the NPN parasitic bipolar transistor which induces a collector current I_C from the drain to the source of the irradiated N-MOSFET.

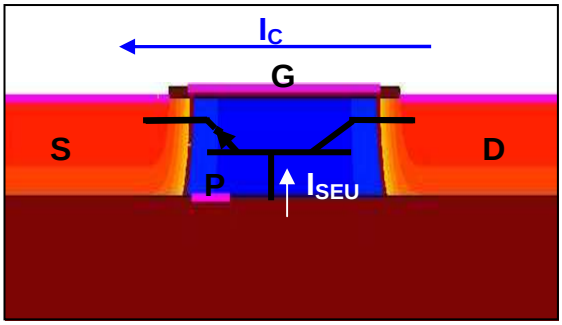

Fig.10: Top view of the SOI N-MOSFET showing the parasitic bipolar transistor.

Fig.10 shows the Verilog-A model connections for the irradiated SOI N-MOSFET. The Verilog-A module provides the single event current I_{SEU} to the NMOS body contact (P).

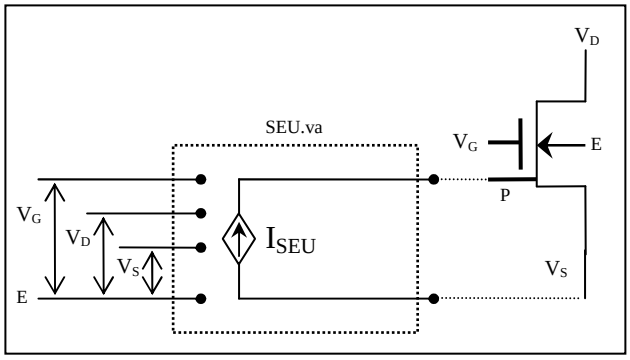

Fig.11 Schematic of Verilog-A model of the SEU for the irradiated SOI NMOS transistor

III.1-Simulation of a Single SOI NMOS Transistor:

ELDO is used to simulate the radiation effects on the OFF SOI N-MOSFET (V_{GS} = 0, V_{DS} = 4V) with the Verilog-A module. The transistor is 1µm long and 6µm wide, similar to the one used in 2D-TCAD and the same energy is considered: LET=30MeV.cm^2/mg

Fig.12 shows the drain current induced by the radiation in the OFF SOI NMOS transistor as a function of time for temperatures of 300, 400 and 500K.

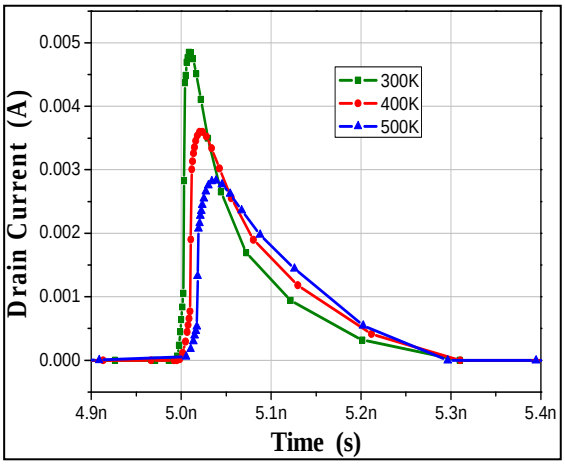

Fig.12: Drain current versus time at temperatures of 300, 400 and 500K induced by LET=0.3pC/ µm

At present, the model does not exactly reproduce the decrease of the peak and the increase of the delay of the induced currents extracted from the 2D-TCAD simulations vs temperature (Tab.1, Tab.2), but the average of the charge induced in the transistor drain is very close (Tab.3) for both simulations. The charge is obviously the main factor responsible for the single event upset of the circuits, as a SEU occurs when a critical value Q_{CRIT} is reached [4]. As the Verilog-A models yield the same charge as 2D-TCAD simulations for the same LET=30MeV.cm^2/mg at different temperatures, we can now rely on the Verilog-A model to simulate the radiation effects on the different circuits.

Temperature (K)	Drain current peak: TCAD (mA)	Drain current peak: Model (mA)
300	4.3	4.84
400	3.1	3.6
500	2.5	2.81

Tab.1: Comparison between the drain current amplitude versus temperature extracted by 2D-TCAD and the Verilog-A model

Temperature (K)	Drain current delay: TCAD (ps)	Drain current delay: Model (ps)
300	140	180
400	193	210
500	250	240

Tab.2: Comparison between the drain current delay versus temperature extracted by the 2D-TCAD and the Verilog-A model

Temperature (K)	Induced charge: TCAD (fC)	Induced charge: Model (fC)
300	359	358
400	360	364
500	361	350

Tab.3: Comparison between the induced charge versus temperature extracted by 2D-TCAD and the Verilog-A model

III.2- Simulation of the SOI CMOS Standard 6T-SRAM cell:

Using the compact Verilog-A model for simulating the radiation effects at different temperatures on the SOI 6T-SRAM cell takes less than 1min per SPICE simulation and yields results very comparable to 2D-TCAD simulations. Fig.13 shows an excellent agreement between the results of LET_th versus temperature for the 6T-SRAM obtained from 2D TCAD simulations and with the compact model, including the reduction of the LET_th slope between 400 and 450K as in the collected charge.

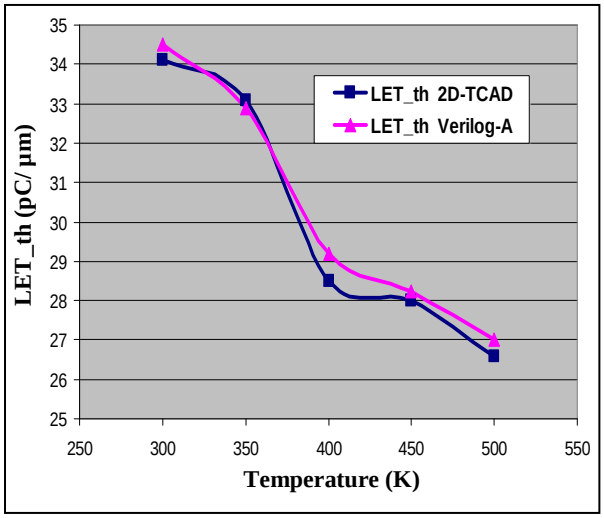

Fig.13 Comparison between the LET_th of the 6T-SRAM versus temperature extracted by the 2D-TCAD and the Verilog_A model

IV. Conclusion

The increase of the temperature from 300 to 500K in radiation environment shows a decrease of the LETth (linear energy transfer threshold) and as a result, an increase of the SEU sensitivity of the 6T-SRAM.

A Spice compact model to simulate the Single Event Effects at different temperatures in SOI CMOS circuits was presented. Comparison between 2D-TCAD mixed-mode and Spice simulations of a 6T-SRAM at different temperature conditions shows a good agreement for our Verilog-A implemented module. This module is less complicated and requires much smaller simulation time compared to 2D-TCAD mixed mode simulations.

Furthermore this model could be extended easily to other circuits simulations. This result is of interest to allow for extensive circuit design studies which cannot be carried out with TCAD physical simulations.

Acknowledgements

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References

[1] L. R. Hite, H. Lu, T. W. Houston, D. S. Hurta, and W. E. Bailey, "An SEU Resistant 256K SOI SRAM", IEEE Transactions on Nuclear Science, December 1992, pp. 2121-2125.

[2] M. L. Alles, L. W. Massengill, S. E. Kerns, K. L. Jones, J. E. Clark, and W. F. Kraus "Effect of Temperature-Dependent Bipolar Gain Distribution on SEU Vulnerability of SOI CMOS SRAMs", 1992 IEEE International SOI Conference Proceedings, pp. 96-97.

[3] W.F. Kraus, B.R. Doyle, J.E. Clark, K. L. Jones, and D.M. Thornberry, "A 20ns Multiple Architecture 256K SIMOX SRAM Designed for harsh Radiation Environments", 1992 IEEE International SOI Conference Proceedings, pp. 168-169.

[4] J.-M. Palau, G. Hubert, K. Coulie, B. Sagnes, M.-C. Calvet, and S. Fourtine, " Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions ", IEEE Transactions on Nuclear Science, vol 48, August 2002, pp. 225-231.

[5] T. Heijmen, D. Giot, and P. Roche, "Factors that impact the critical charge of memory elements", On-Line Testing Symposium, 12th IEEE International IOLTS, 2006, pp 6

[6] R. Naseer, Y. Boulghassoul, J.Draper, S. DasGupta, and A. Witulski "Critical Charge Characterization for Soft Error Rate Modeling in 90nm SRAM", IEEE International Symposium on Circuits and Systems, ISCAS 2007 , pp 1879 – 1882

[7] D. Truyen, J. Boch, B. Sagnes, N. Renaud, E. Leduc, S. Arnal, and F. Saigné, "Temperature Effect on Heavy-Ion Induced Parasitic Current on SRAM by Device Simulation: Effect on SEU Sensitivity", IEEE Transactions on Nuclear Science, vol. 54, No. 4, August 2007, pp. 1025 - 1029

[8] J. G. Rollins and J. Choma, "Mixed-mode PISCES-SPICE coupled circuit and device solver, " IEEE Transactions on computer-aided design, vol. 7, pp. 862-867, Aug. 1988.

[9] R.L Woodruff and P.J. Rudeck; "Three-Dimensional Numerical Simulation of Single Event Upset of an SRAM Cell", IEEE Trans. Nuclear. Science, vol. 40, No. 6, pp. 1795-1803, December 1993.

[10] P.J. McNulty, P. Roche, J.M. Palau, and J. Gasiot, "Threshold LET for SEU induced by low energy ions [in CMOS memories]", IEEE Transactions on Nuclear Science, vol 46, December 1999, pp. 1370 - 1377.

[11] Sentaurus Device User, GuideVersion Z-2007.03.

[12] D. Truyen, J. Boch, B. Sagnes, J.-R. Vaillé, N. Renaud, E. Leduc, M. Briet, C. Heng, S. Mouton, and F. Saigné, "Temperature Effect on Heavy-Ion-Induced Single-Event Transient Propagation in CMOS Bulk 0.18 µm Inverter Chain", IEEE Transactions on Nuclear Science, vol. 55, No. 4, pp. 2001-2006, 30 September 2008.

[13] P. Roche, J. M. Palau, G. Bruguier, C. Tavernier, R. Ecoffet, and J. Gasiot, "Determination of key parameters for SEU occurrence using 3-D full cell SRAM simulations," IEEE Trans. Nucl. Sci., vol. 46, no. 6, pp. 1354–1362, Dec. 1999.

[14] J.-M. Palau, G. Hubert, K. Coulié, B. Sagnes, M. C. Calvet, and S. Fourtine, "Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions," IEEE Trans. Nucl. Sci., vol. 48, no. 2, pp. 225–231, Apr. 2001.

[15] Castellani-Coulie, K.; Palau, J.-M.; Hubert, G.; Calvet, M.-C.; Dodd, P.E.; Sexton, F.; "Various SEU conditions in SRAM studied by 3-D device simulation", IEEE Trans. Nucl. Sci., vol. 48, no. 6, pp. 1931–1935, Dec. 2001

[16] J.G. Rollins and J. Choma, Jr., "Mixed-Mode PISCES-SPICE coupled circuit and device solver", IEEE Trans. Computer Aided Design., vol. 7, No. 8, pp. 862-867, 1988.

[17] R.L Woodruff and P.J. Rudeck; "Three-Dimensional Numerical Simulation of Single Event Upset of an SRAM Cell", IEEE Trans. Nucl. Sci., vol. 40, No. 6, pp. 1795-1803, December 1 993.

[18] Merelle, T.; Chabane, H.; Palau, J.-M.; Castellani-Coulie, K.; Wrobel, F.; Saigne, F.; Sagnes, B.; Boch, J.; Vaille, J.R.; Gasiot, G.; Roche, P.; Palau, M.-C.; Carriere, T.; "Criterion for SEU Occurrence in SRAM Deduced From Circuit and Device Simulations in Case of Neutron-Induced SER", IEEE Trans. Nucl. Sci., vol. 52, no. 4, pp. 1148–1155, Aug. 2005.

[19] Naseer, R.; Boulghassoul, Y.; Draper, J.; DasGupta, S.; Witulski, A.; "Critical Charge Characterization for Soft Error Rate Modeling in 90nm SRAM" Circuits and Systems, IEEE International Symposium ISCAS 2007, pp. 1879 - 1882

[20] J. Alvarado, V. Kilchytska, E. Boufouss and D. Flandre, "Modeling of Single Event Transients and Total Dose in Partially Depleted SOI CMOS Circuits", EuroSOI workshop 2010.