A DC-120 GHz SPDT Switch Based on 22 nm FD-SOI SLVT NFETs with Substrate Isolation Rings Towards Increased Shunt Impedance

M. Rack, L. Nyssens, Q. Courte, D. Lederer, J.-P. Raskin
Université catholique de Louvain, Belgium
martin.rack@uclouvain.be

***Abstract*— A DC-120 GHz SPDT switch is proposed using GlobalFoundries' 22FDX® SLVT devices with improved substrate isolation rings. For mm-wave switch applications, 22FDX® offers BFMOAT devices that include substrate isolation zones *beneath* them to reduce high-frequency shunt loss, though, compared to SLVT devices, this sacrifices the back-gate functionality, resulting in higher $R_{on}C_{off}$. This paper proposes and analyses substrate isolation zones implemented in ring-shapes *around* SLVT-FETs to reduce parasitic shunt admittance while preserving the back-gate. The resulting effective device boasts a low $R_{on}C_{off}$ metric (thanks to an SLVT-FET core with back-gate) and simultaneously achieves high substrate impedance to the reference ground node (similar performance as BFMOAT-FETs). From such devices, a full SPDT switch was fabricated and characterized up to 130 GHz. Having less than 2.4 dB insertion loss and better than 22 dB isolation from DC to 120 GHz, it outperforms analogous SPDT modules implemented using conventional SLVT or BFMOAT FETs.**

***Keywords*— $R_{on}C_{off}$, shunt parasitic loss, switch, SPDT, ultra-wideband, millimetre-wave IC, 5G front-end, FD-SOI, UTBB.**

I. Introduction

The well-known transistor figure of merit for RF switch applications is the $R_{on}C_{off}$ product. At RF frequencies (i.e., below a few tens of GHz), the *series* terms R_{on} and C_{off} are quite sufficient to describe a device technology for switch applications. Shunt capacitance C_{sh} terms can be neglected at RF (since $j\omega C_{sh}$ is quite low), and parasitic C_{sh} can be compensated for using passive matching circuits. This is not the case for any shunt conductance terms G_{sh}, that will always be a source of additional degradation in switch insertion loss (IL), regardless of any passive matching scheme.

In the 22FDX® node from GlobalFoundries, the SLVT device presents an $R_{on}C_{off}$ metric of the order of 100 fs [1,2], but is outperformed by the BFMOAT device for mm-wave switch applications [2,3,4], even though the BFMOAT's $R_{on}C_{off}$ is substantially higher at around 160 fs.

The origin of BFMOAT's higher performance results at high frequencies was explained in [4], where *shunt* parasitic terms were shown to contribute to FET performance (insertion losses). The importance of shunt loss was demonstrated by analyzing how a BFMOAT device outperforms an SLVT as a mm-wave switch despite having a significantly larger $R_{on}C_{off}$. Compared to the SLVTs, BFMAOT FETs forgo below-BOX implants over the entirety of the active device area in order to increase substrate impedance to/from the FET. The back-gate functionality is then sacrificed, which is why the R_{on} of the BFMOAT cannot reach an as low a value of that of the SLVT.

In this paper, we propose implementing a BFMOAT ring *around* an SLVT device to substantially increase substrate impedance to the FET while *maintaining the back-gate* access. In this manner, a device with simultaneous low $R_{on}C_{off}$ and with high shunt resistance up to mm-wave frequencies is achieved. Using such a FET with BFMOAT ring layout, an ultra-wideband DC-120 GHz SPDT is implemented with low loss, that outperforms an analogous switch implemented using BFMOAT FET devices thanks to the lower $R_{on}C_{off}$ metric.

II. Shunt Loss Analysis

A. SLVT vs. BFMOAT

As illustrated in Fig. 1, the SLVT incorporates a back-gate (BG) electrode below the thin (20 nm) buried oxide (BOX).

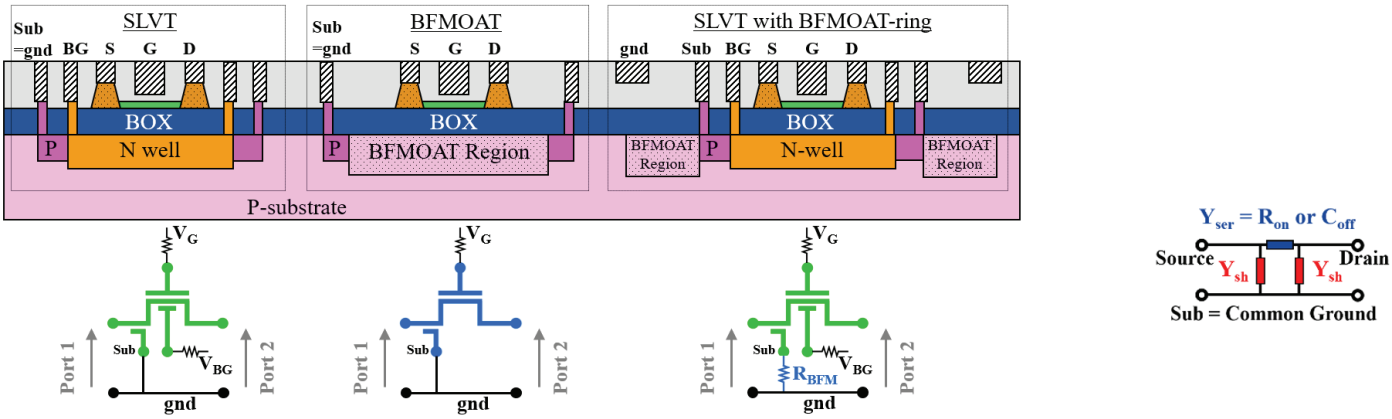

Fig. 1. Simple representation of different types of FD-SOI NFETs: SLVT, BFMOAT and SLVT with BFMOAT-ring, and two-port equivalent circuit pi-model.

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Applying a positive bias to the BG results in a more conductive channel in the on-state and to a lower value of R_{on}. The BFMOAT device sacrifices the BG functionality for reduced shunt losses G_{sh} to the ground reference node. Both devices include a P-type substrate-tap ring ("Sub" node in Fig. 1) to include shunt parasitics in the mm-wave models.

To highlight the impact of $R_{on}C_{off}$ and G_{sh}, single FETs are simulated in two-port configuration between source and drain.

The gate and BG are biased through large resistors, and these nodes can be considered as RF floating. Both FETs are 20 nm long, are referenced to the C3 (5^{th}) metal layer, and have five fingers ($N_f = 5$), each with a width of $W_f = 5$ µm.

Fig. 2 plots the on- and off-state results pertaining to each FET. It plots the S-parameters and equivalent circuit elements of the two-port pi-model (see Fig. 1). The on-state is set by applying 0.9 V to the gate (V_g) and 3 V to the back-gate (V_{bg}), while in the off-state V_g = -0.9 V and V_{bg} = 0 V.

The R_{on} element (extracted as $\Re\{-1/Y_{21}\}$) determines the low frequency loss, however the real part of the shunt admittance $G_{sh} = \Re\{Y_{sh}\}$ increases with frequency and is responsible for substantial additional loss in the SLVT device, where $Y_{sh}=Y_{11}-Y_{21}$ (=$Y_{22}-Y_{21}$ in a symmetrical device). This is demonstrated in Fig. 2c which shows that S_{21} appreciably decreases above ~30 GHz. Fig. 2e shows that the power transfer coefficient $|S_{21}|^2$ reduces by 11% over the considered frequency range, and that only 2% of this is due to reflection by increased mismatch (see $|S_{11}|^2$). This indicates that the $|S_{21}|^2$ reduction is mainly attributable to loss increase in the network.

Fig. 2g shows that the G_{sh} term of the BFMOAT device saturates at a value of around 160 µS, which it reaches at around 30 GHz. This explains the 1% degradation in $|S_{21}|^2$ at 30 GHz. The SLVT's G_{sh} term reaches 1 mS at 110 GHz, and continues to increase with frequency. This term is responsible for the 9% increase in power loss in the SLVT at 110 GHz.

In [4] a formulation for shunt-loss-FoM to complement the series-$R_{on}C_{off}$-FoM was described. The factor K accounts for the loss dissipated in the G_{sh} term, and is expressed as follows, where Y_0 is the reference port impedance in the system:

$$K = Y_0/(Y_0+G_{sh}) \quad (1)$$

Accurate equivalent circuit extraction of the considered SLVT and BFMAOT devices can be obtained based on the simple lumped pi-model described in Table 1.

This simple model fits well to the simulated full PDK models, and demonstrates the impact of the real part of the shunt admittance on the overall loss in the two FETs (R_s = 5.5 kΩ for the BFMOAT and 82 Ω for the SLVT). High values of R_s are desirable to avoid large shunt loss factors K.

B. SLVT with BFMOAT-Shunt-Impedance-Enhancing Ring

The effective shunt resistance to ground can be increased by adding some series impedances between the Sub node of the devices and the common RF ground. This scheme is depicted in Fig. 1, where an SLVT device is proposed with a BFMOAT isolation ring defined *around* it, that will add some R_{BFM} term toward the ground node.

Fig. 2 includes simulations of SLVT devices with such additional R_{BFM} elements introduced with values of 1 kΩ, 5 kΩ and 1 MΩ. The results show that the $S_{21\text{-}ON}$ data pertaining to a 1 MΩ R_{BFM} achieve the lowest overall loss over the whole band, since: (i) the R_{on} is low thanks to the inherent performance of a back-gate-biased SLVT core, and (ii) since the overall G_{sh} term is made extremely low for R_{BFM} = 1 MΩ. When R_{BFM} is set to 5 kΩ, a small degradation in IL ($S_{21\text{-}ON}$ curves) is observed at around 6.7 GHz but the degradation is not severe (K factor of around 0.08 dB). The frequency at which this transition occurs, and the amplitude of the degradation are similar to those observed for the regular BFMOAT device (K=0.07 dB). However, the low-frequency loss in the BFMOAT FET is higher due to a larger-valued R_{on}. The simulation employing an R_{BFM} of 1 kΩ shows quite a substantial degradation, with a K factor of 0.39 dB. A 1 kΩ value is then not considered high enough for comfortable operation. It is interesting to note that using an R_{BFM} value of 1 kΩ results in an effective device that outperforms the regular SLVT above approximately 80 GHz, but actually has more loss below 80 GHz. This is due to the transition frequency being pushed higher for lower values of R_s. This is highlighted

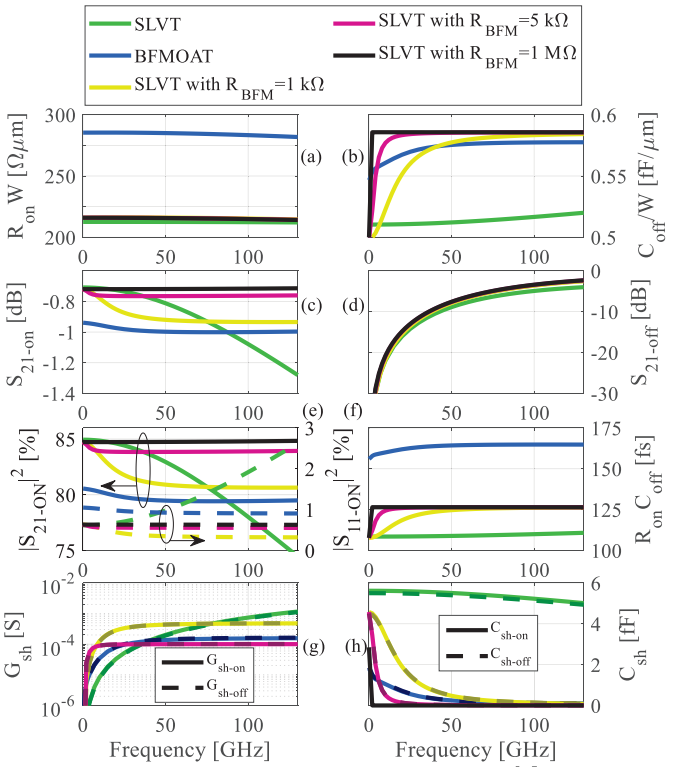
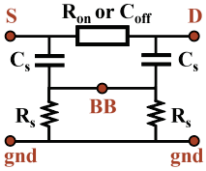


Fig. 2. Loss and pi-model analysis of SLVT and BFMOAT FETs simulated in two-port (switch) configuration (Fig. 1) in both ON and OFF states. All FETs are referenced to the C3 (5^{th}) metal plane and have W_f = 5 µm, N_f = 5 (total width $W = N_fW_f$ = 25 µm).

Table 1. Analysis of on-state FETs as switches

Model		Equiv.-circuit			Performance	
FET	R_{BFM} [Ω]	R_{on} [Ω]	C_s [fF]	R_s [Ω]	K [dB] (at $f \gg f_s$)	f_s [GHz]
BFMOAT	0	11.4	1.7	5530	-0.07	16.9
SLVT	0	8.5	4.7	82	-4.1	413
SLVT	1 k	8.5	4.7	1082	-0.39	31.3
SLVT	5 k	8.5	4.7	5082	-0.08	6.7
SLVT	1 M	8.5	4.7	1 M	-0.0004	0.03



in Table 1, that lists the overall R_s and C_s for all equivalent FETs, as well as giving the degradation K value and the frequency at which the full degradation occurs (i.e. the high frequency at which the overall loss becomes frequency-independent), when voltage begins to drop over R_s as it starts to dominates over ωC_s:

$$f_s = 1/(2\pi R_s C_s) \quad (2)$$

Though the degradation is more severe at high-frequency when R_{BFM} is zero, it only appears at frequencies which are relatively high. Therefore, when working below a few GHz, not adding any shunt resistive elements is the better choice.

Fig. 2b illustrates that the C_{off} metric of the effective device is influenced by the shunt impedance value of R_{BFM}. This impacts directly the series-FoM of $R_{on}C_{off}$ (Fig. 2f), and the SLVT devices with increased shunt impedance elements demonstrate a 15% increase in C_{off} and in $R_{on}C_{off}$. This phenomenon can be explained based on an analysis of the equivalent circuit of Table 1. As the elements R_s tends to a short circuit (case for the usual SLVT device), the below-BOX node BB tends to an RF ground, and both C_s elements contribute to pure shunt admittance. In that case (R_s very low), the Y_{21} parameter of the network becomes:

$$Y_{21} = -j\omega C_{off} \qquad \text{for } R_s \approx 0 \quad (3)$$

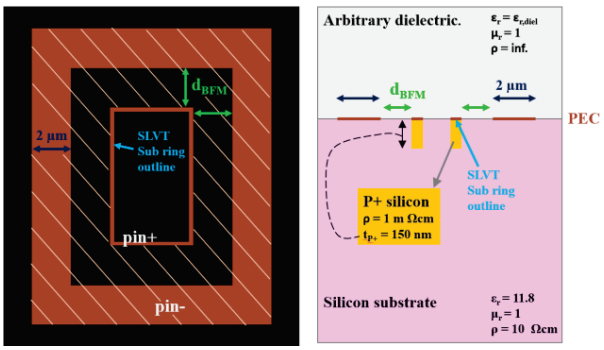
The series capacitance between source and drain extracted from Y_{21} is then simply the C_{off} term related to the device network mainly above the BOX. However, as the R_s elements tends to an open circuit (case for the usual BFMOAT device and for the SLVT devices with an added R_{BFM} term), the BB node becomes floating from the reference ground node, and $C_s/2$ is effectively seen in parallel with C_{off}, as the Y_{21} parameter of the network then becomes:

$$Y_{21} = -j\omega(C_{off} + C_s/2) \qquad \text{for } R_s \approx +\infty \quad (4)$$

The effective C_{off} is then increased by $C_s/2$. Despite the resulting 15% increase in the $R_{on}C_{off}$ FoM when adding a large R_{BFM} term to the SLVT device, the benefits in shunt loss for mm-wave applications are worthwhile. In that case, notice that the C_{off} value is very close to that of the regular BFMOAT device, whose BB node is similarly isolated in the same way.

The analysis performed above suggests that substrate resistances of at least 5 kΩ to ground should be targeted for mm-wave switches. To evaluate the impedance of a BFMOAT ring placed around an SLVT device, EM simulations are run to extract the value of the equivalent R_{BFM} element (see Fig.1).

The substrate tap-ring of the studied SLVT device (W_f = 5 µm and N_f = 5) is depicted as the inner PEC (perfect electrical conductor) ring in Fig. 3a, and a first pin; named pin+, is defined on that ring. A P+ substrate-plug is defined directly below the ring, with equivalent depth and resistivity of 150 nm and 1 mΩcm. A second PEC ring (2 µm-wide) is defined around the first, at a uniform distance labelled as d_{BFM}. This outer-ring represents the RF reference ground plane. A second pin, named pin-, is defined on this outer ring. A single port is defined between pin+ and pin-, and the EM simulation is run on the material stack of Fig. 3b, comprised of a 10 Ωcm silicon substrate with a permittivity $\varepsilon_{r,Si}$ of 11.8, and of an



(a) (b)

Fig. 3. EM simulations run to obtain the substrate impedance between two coplanar electrode rings. (a) Top view of the physical layout (hashed regions are BFMOAT zones of 10 Ωcm). (b) Vertical view of the material stack.

arbitrary dielectric layer of permittivity $\varepsilon_{r,diel}$. As depicted in Fig. 3b, the PEC electrode pin shapes are defined in between these two semi-infinite materials.

From the simulated Y_{11} results, the parallel substrate resistance R_{BFM} and capacitance C_{BFM} are computed as:

$$R_{BFM} = 1/\Re\{Y_{11}\} \quad (5)$$

$$C_{BFM} = \mathcal{I}\{Y_{11}\}/\omega \cdot \varepsilon_{r,Si}/(\varepsilon_{r,Si}+\varepsilon_{r,diel}) \quad (6)$$

Results of C_{BFM} and R_{BFM} are flat over frequency, and their values are plotted in Fig. 4 versus the d_{BFM} parameter. The results show that an R_{BFM} value above 5 kΩcm is achievable using a BFMOAT isolation ring width of 1.7 µm. This correlates well to the size extent of the BFMOAT shapes used in usual BFMOAT-FETs. From these results, SLVT devices with 2 µm-wide substrate isolation rings were designed with which to implement a DC-120 GHz SPDT switch.

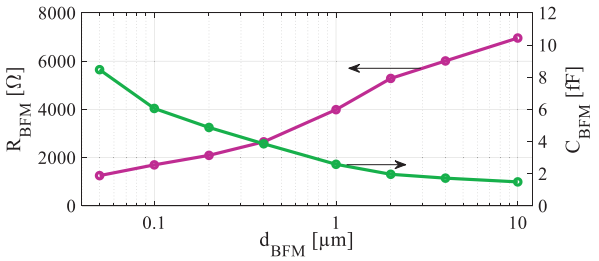


Fig. 4. EM-simulation results of R_{BFM} and C_{BFM} vs. BFMOAT ring width.

III. A DC-120 GHz SPDT Switch

To demonstrate the device's performance for high mm-waves, a wideband SPDT switch was designed, fabricated and measured based on the series-shunt topology (Fig. 5). One port of the SPDT is loaded on-chip with a 50 Ω resistor.

The design is a re-used one that was based on BFMOAT-FETs [4], in which all BFMOAT FETs have been replaced by SLVT devices with a 2 µm-wide substrate isolation ring to RF ground. The initial design was performed to achieve minimal on-state IL while maintaining at least 20 dB of isolation in the off-state at 80 GHz based on the BFMOAT FET. Including EM post-layout simulations and open-pad de-embedding, this was achieved during the design for the following choice of parameters [4]: $W_{f\text{-}ser} = W_{f\text{-}sh} = 3$ µm and $N_{f\text{-}ser} = N_{f\text{-}sh} = 15$. The gate lengths of all FETs were set to the minimum of 18 nm.

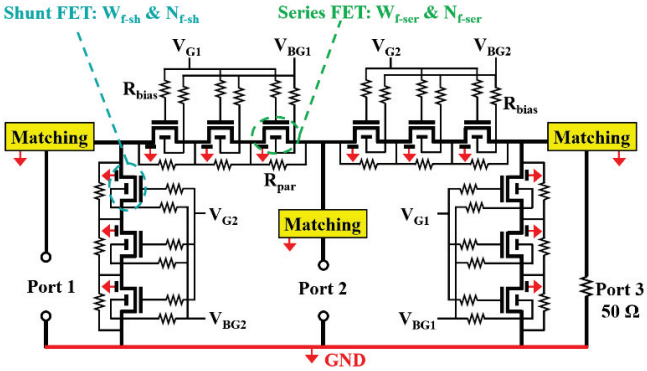


Fig. 5. Series-shunt SPDT topology. 3-stacked FETs target P_{1dB} > 20 dBm.

The SPDT switches were fully characterized under small-signal conditions using an on-wafer set-up up to 130 GHz, and the S-parameter results are plotted in Fig. 6. The BFMOAT-FET-design achieved the desired performances, showing good operation over the DC-80 GHz band [4].

By substituting the BFMOAT FETs for the isolated SLVTs, a clear gain in performance is observed. Thanks to the R_{on}, there is less IL and better isolation over the entire band, and instead of the IL experiencing strong roll-off starting from 70 GHz, it remains steady, below -2.4 dB, up to 120 GHz. The P_{1dB} is also improved, as is expected when using the back-biased SLVT device with lower V_{th} than the BFMOAT [3].

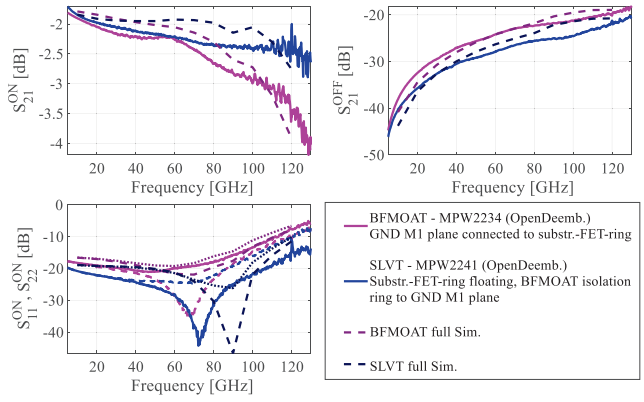


Fig. 6. Simulated and measured $S_{ij\text{-}on}$ and $S_{ij\text{-}off}$ of the fabricated SPDTs.

Good agreement is achieved between the post-layout simulations and the measured data for both SPDT switches.

Table 2 benchmarks these results against the published state-of-the-art SPDT switches covering frequencies close to 100 GHz, and demonstrates the competitiveness of the presented DC-120 GHz SVLT-based series-shunt switch.

IV. Conclusion

For low-loss mm-wave switch applications, BFMOAT devices offer high shunt impedance values to a reference substrate pin by sacrificing the below-BOX back-gate implants. Compared to the SLVT device, this approach highly mitigates shunt loss, but this comes at the price of a degraded series-$R_{on}C_{off}$-FoM of 160 fs, compared to 100 fs in the SLVT.

This paper proposes using a BFMOAT implant-blocking ring *around* SLVT devices without affecting the below-BOX regions beneath the active area to retain the back-gate contact.

Device models (PDK) and EM simulations (to evaluate 3D substrate impedance) were employed to demonstrate how this solution yields an effective device that simultaneously achieves high substrate shunt impedance and a low $R_{on}C_{off}$. The effective $R_{on}C_{off}$ was slightly degraded (15%) by isolating the below-BOX region beneath the FET. The dependency of C_{off} on the shunt impedance value was explained, and is a worthwhile trade-off for mm-wave switch applications.

To demonstrate the performance of the proposed arrangement, broadband SPDT switches were designed and measured based on a series-shunt topology. Two SPDTs were fabricated, the first based on BFMOAT devices, and the second on SLVT devices with resistive substrate isolation rings. Measurements and simulations clearly demonstrate the advantage of the latter SPDT switch over the former, which is attributed to the two types of FET having similar shunt performance, while the SLVT-based devices retain their inherently better $R_{on}C_{off}$-series FoM.

Overall, an ultra-broadband SPDT switch module was achieved, with less than 2.4 IL and better than 22 dB isolation up to 120 GHz, for up to 20 dBm of RF power handling.

Table 2. State-of-the-art SPDT switches operating close to 100 GHz.

Work	Techno.	Topology	Freq. [GHz]	Insertion Loss [dB]	Isolation [dB]	Area [10^{-3} mm²]
[5]	65 nm CMOS	Traveling Wave	17-100	2.8-4.5	> 15	420 $^{\$}$ 200 **
[6]	180 nm SiGe	Transform.	90	2.7	14	43 *
[7]	800 nm InP	λ/4-Shunt	90-170	3.0-5.0	42-55	650 **
[8]	100 nm GaN	λ/4-Shunt	68-134	1.1-2.1	17.6-21.5	308 *
[9]	50 nm InGaAs	λ/4-Shunt	50-75	1.0-1.6	31.6-32.8	348 *
			72-110	1.0-1.6	28.5-31.4	216 *
[4] This	22 nm FD-SOI	Series-Shunt	DC-80	< 2.6	> 22	14 *
			DC-120	< 2.4	> 22	14 *

*Excluding pads $^{\$}$Including pads. **Estimate excluding pads.

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