IEEE Benelux General assembly

Meet the fellows

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High Resistivity SOI substrates boost CMOS RF performance

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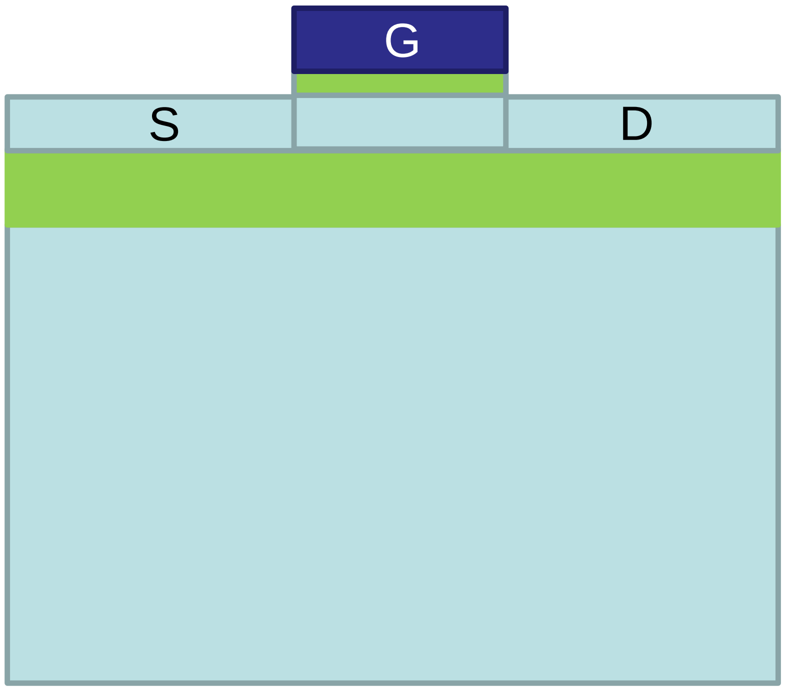
A large diversity of SOI wafers



Top Si 10 nm … 50 µm

BOX 25 nm … 2 µm

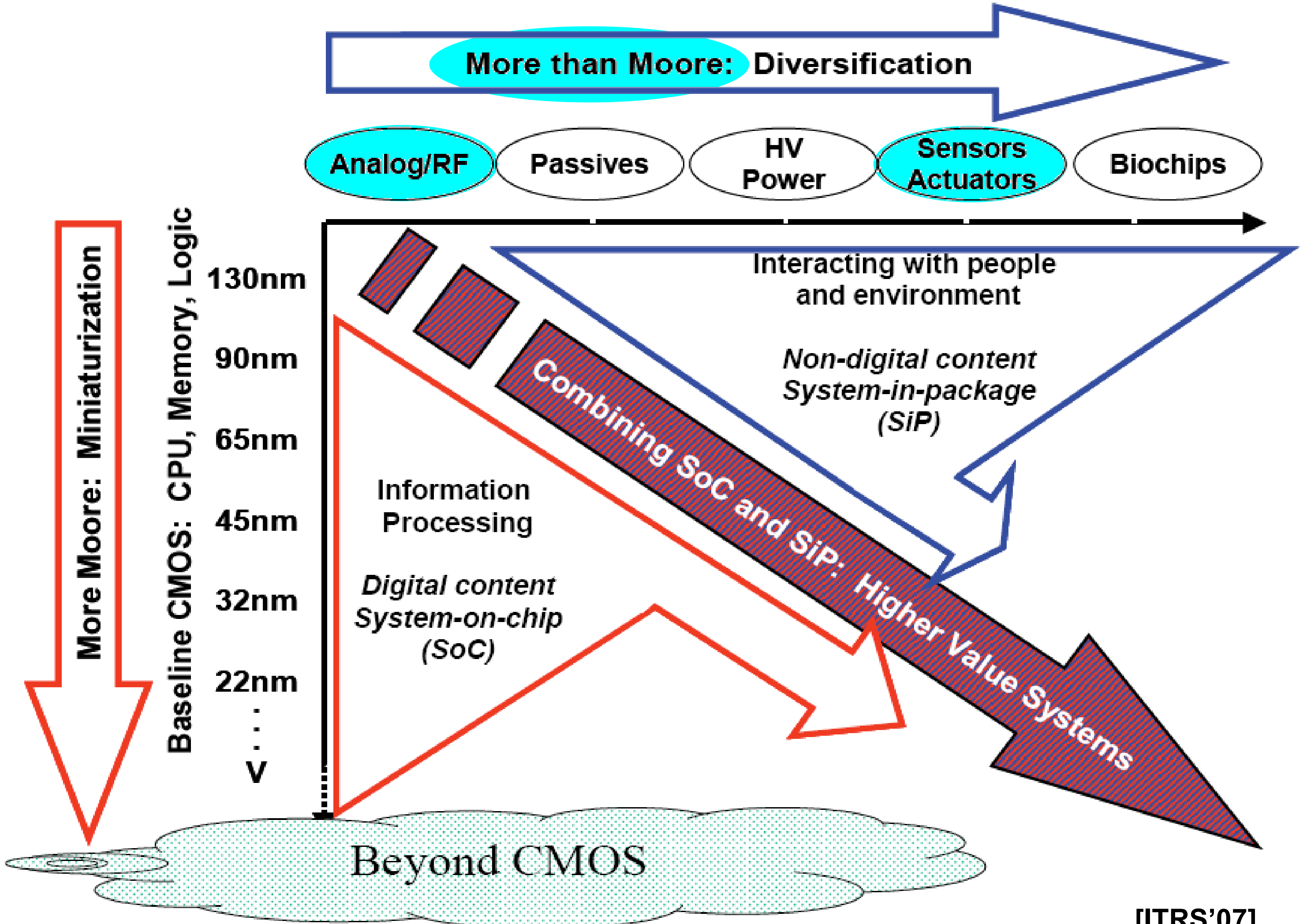
Handle Si substrate 300 µm … 1 mm

Resistivity: 10 Ω.cm … 10 kΩ.cm

CMOS technologies

RF SOI: Si around 100 nm, BOX: 145 nm, 400 nm, 1 µm

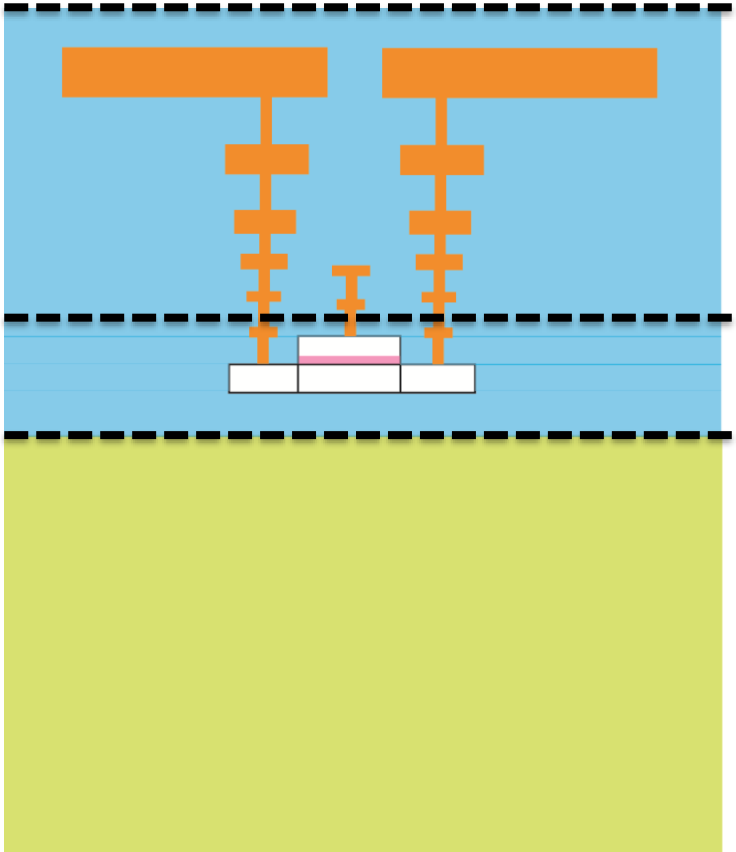
UTBB: Si: 10 nm, BOX: 25 nm



[ITRS'07]

UCL Université catholique de Louvain

RF SOI CMOS – challenges at different levels…



Back-end

RC parasitics – thick metal, CNTs, low-k

Front-end – new materials, transistors

Substrate

Losses, crosstalk, thermal issues, linearity, …

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RF SOI MOSFETs: State-of-the-Art

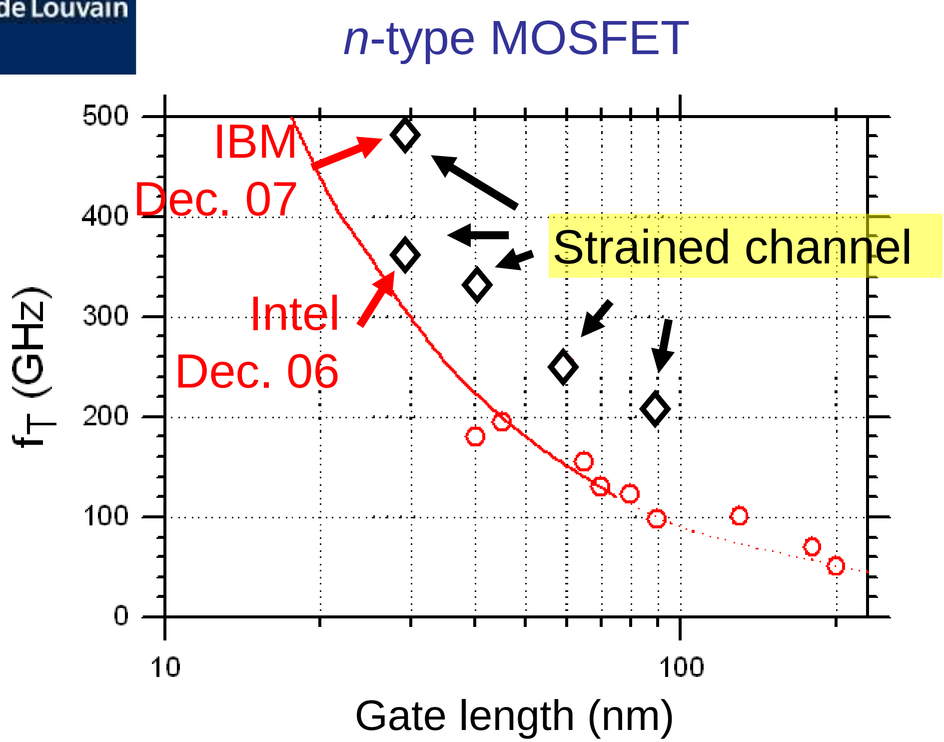
CMOS down scaling

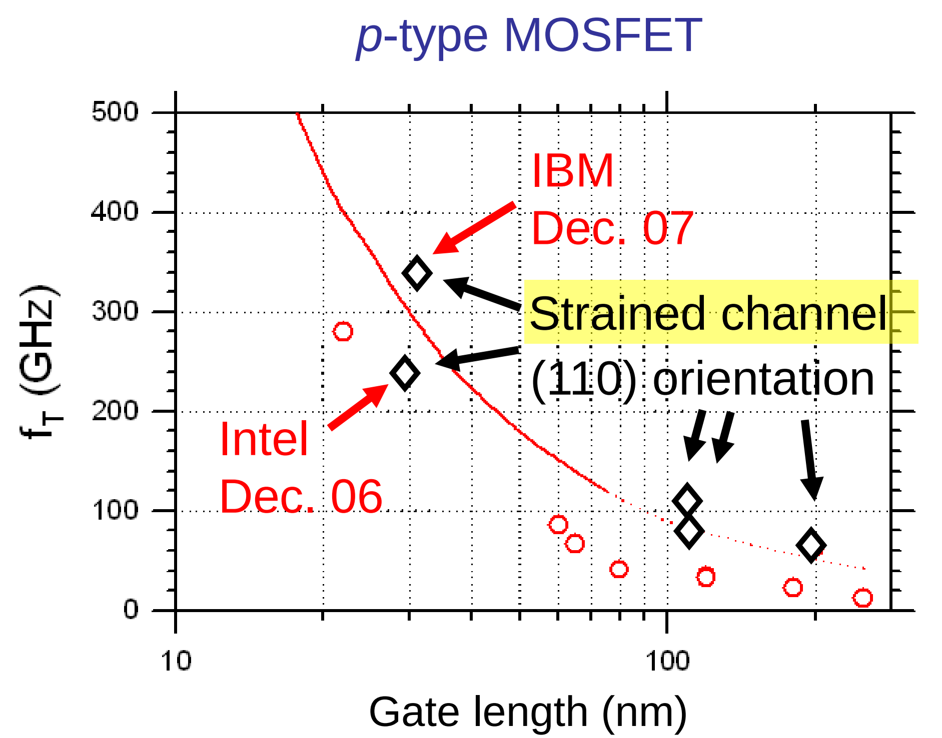
1990	1995	2000	2005	2010
PD/FD SOI	Silicidation	High-k Metal gate	Strained channel	Multiple gate

Operating frequency increase

RF MOSFET performance: State-of-the-Art

Cut-off frequency of the current gain (i_d/i_g): f_T





→ *IBM: record RF performance of **sub-45 nm** SOI CMOS (2007)*
Peak f_T of 485 GHz and 345 GHz measured in floating-body nFET and pFET

Complementary MOS (CMOS)

[R. Valentin, IEMN, PhD thesis]

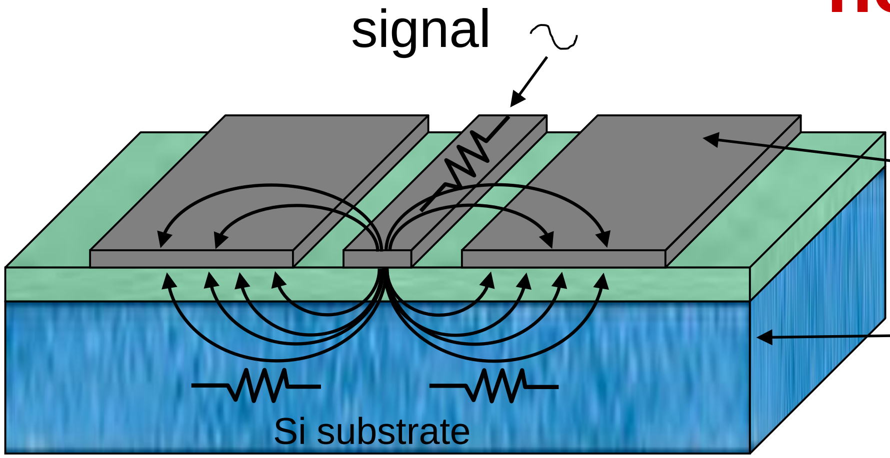
RF SOI substrate: State-of-the-Art

Wafer scale up

1992	1997	2005	2012
SOITEC Smart cut	HR SOI (UCL)	Trap-rich SOI (UCL)	eSI substrate (SOITEC & UCL)

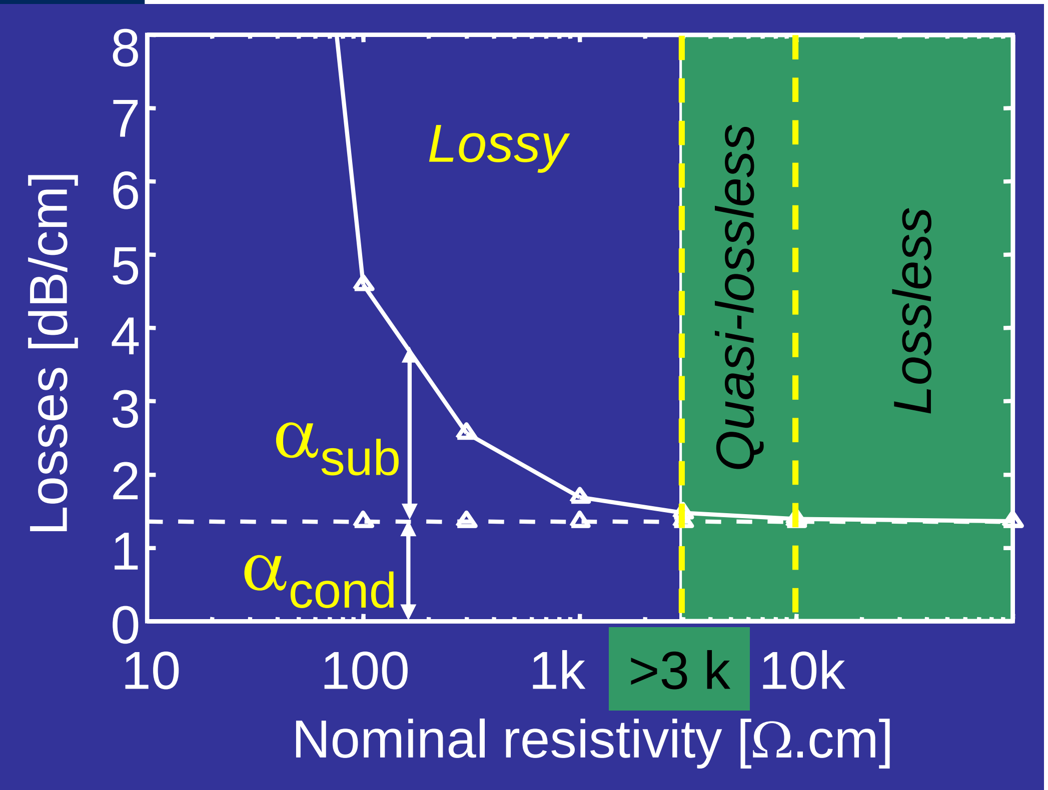
Substrate resistivity increase

High Resistivity SOI substrates: how high should we go?



Conductor losses (α_{cond})

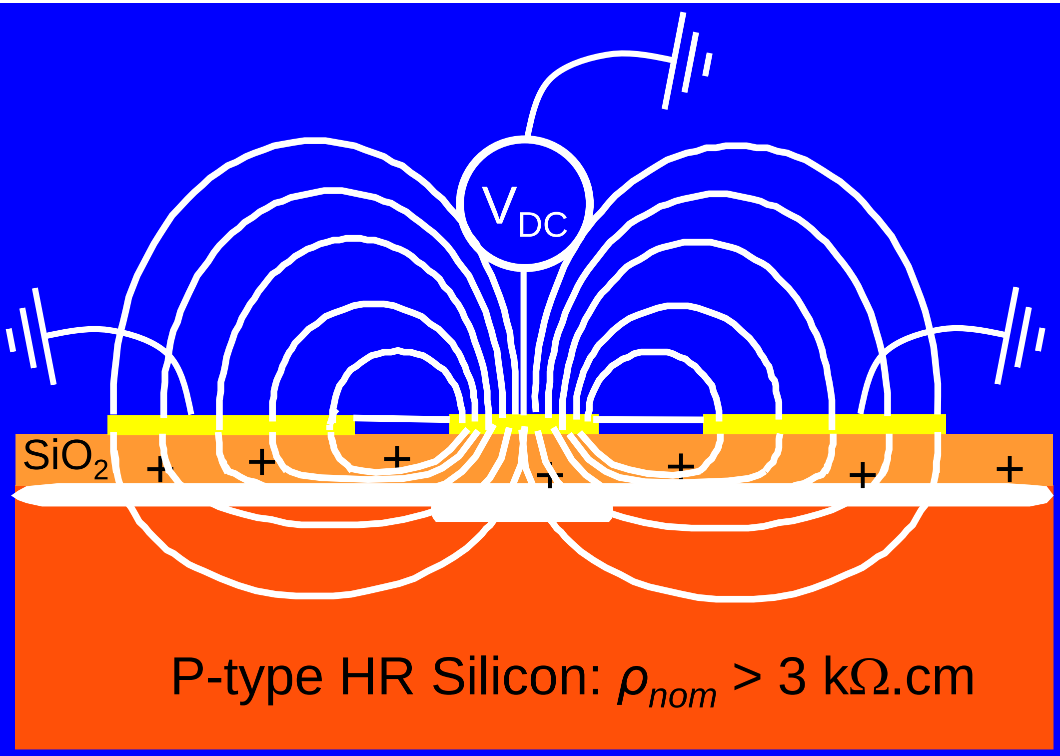
Substrate losses (α_{sub})



- STD SOI: 20 Ω.cm ⇒ high losses

- HR SOI of 10 kΩ.cm would correspond to a lossless Si substrate

Parasitic Surface Conduction (PSC)



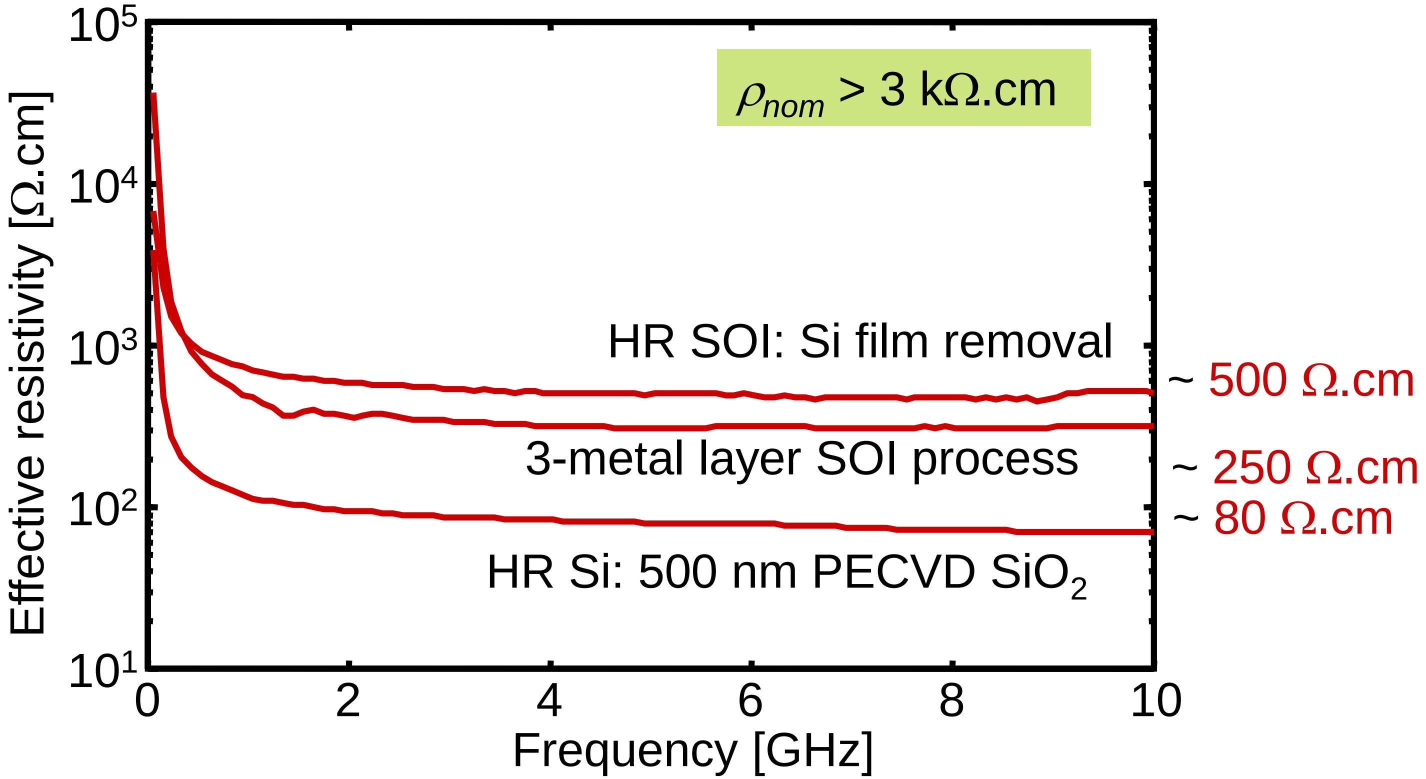
PSC caused by:

- fixed charges (Q_f) in the oxide (BOX of SOI, IMD layers)
- Bias applied on the metallic conductors

For oxidized HR Si:

- *Effective* resistivity lower than *nominal* resistivity
- Substrate losses higher than expected (coplanar devices)

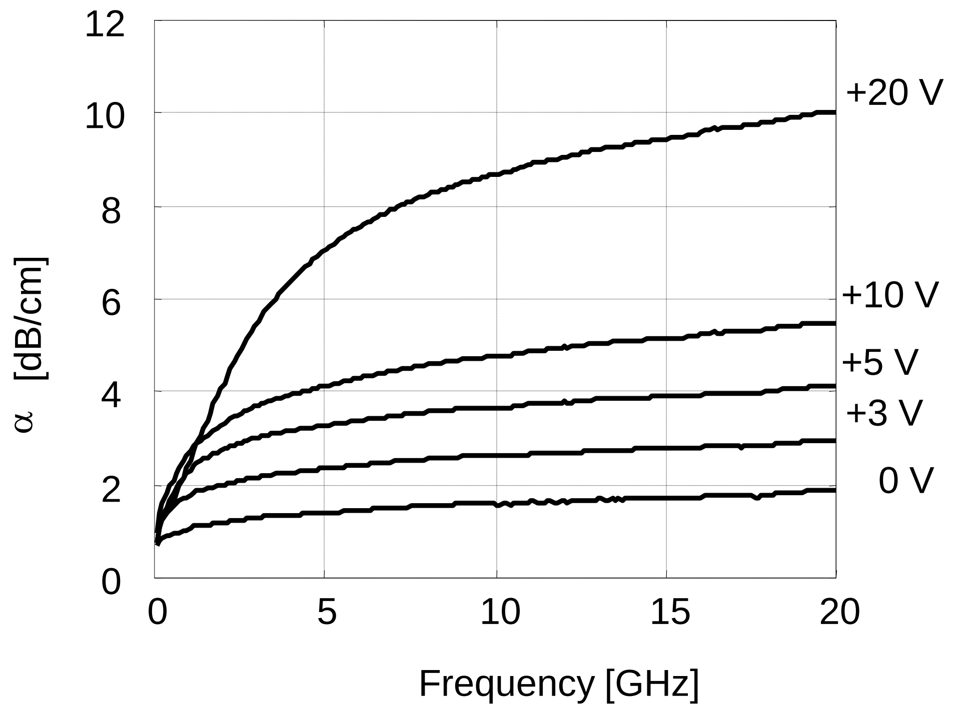
Typical ρ_{eff} values



- Effective resistivity depends on process
- Effective resistivity is lower than 1 kΩ.cm

[D. Lederer, J.-P. Raskin, *IEEE EDL'05*]

Transmission lines on SOI vs DC bias

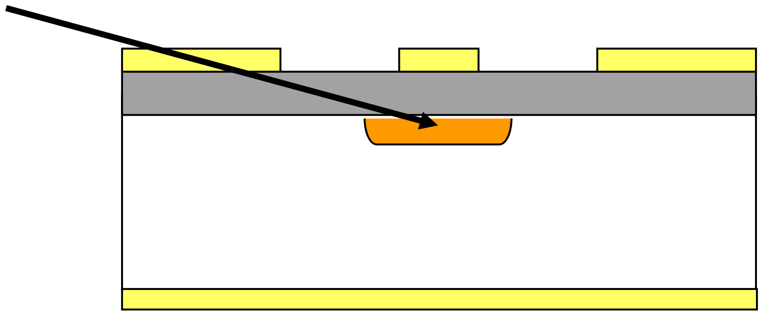


MEMS applications

|V_a| increases the line losses:

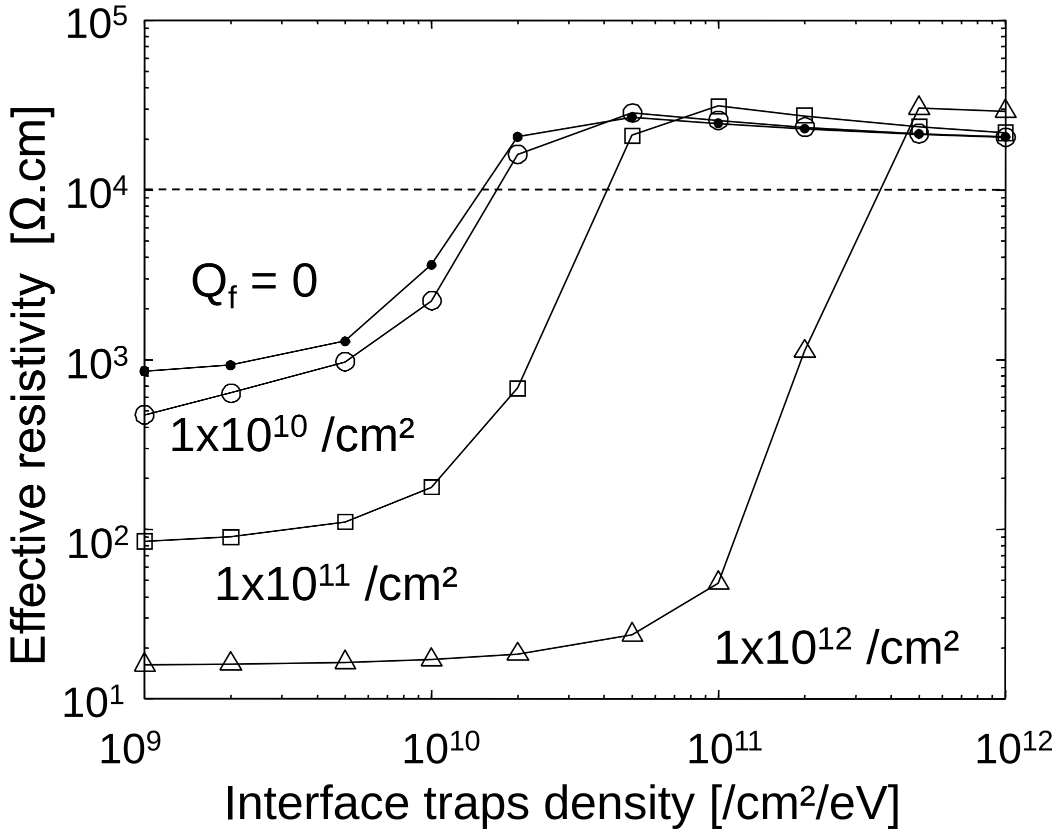
- Accumulation or inversion of carriers below the field oxide

- Reduction of ρ_{eff} (seen by the lines)



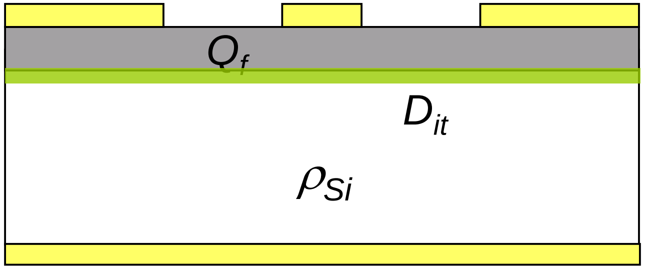
Dependence of the effective resistivity

$$\rho_{eff} = f\,(\,\rho_{Si}\,,\,Q_f\,,\,t_{ox}\,,\,V_a\,,\,D_{it}\,)$$

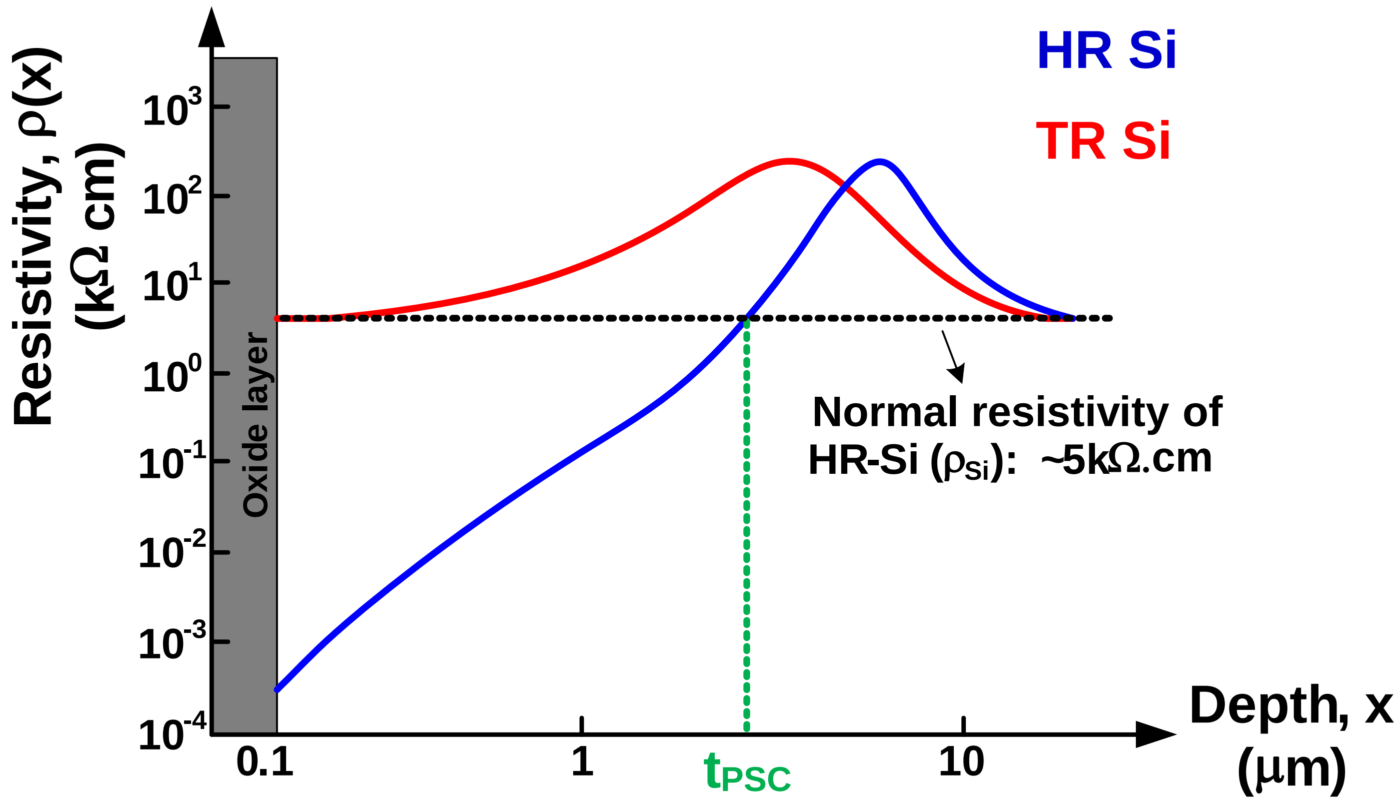


D_{it} ~ 10^{12} /cm²/eV

for being independent
on Q_f, and then reach
the high resistivity behavior



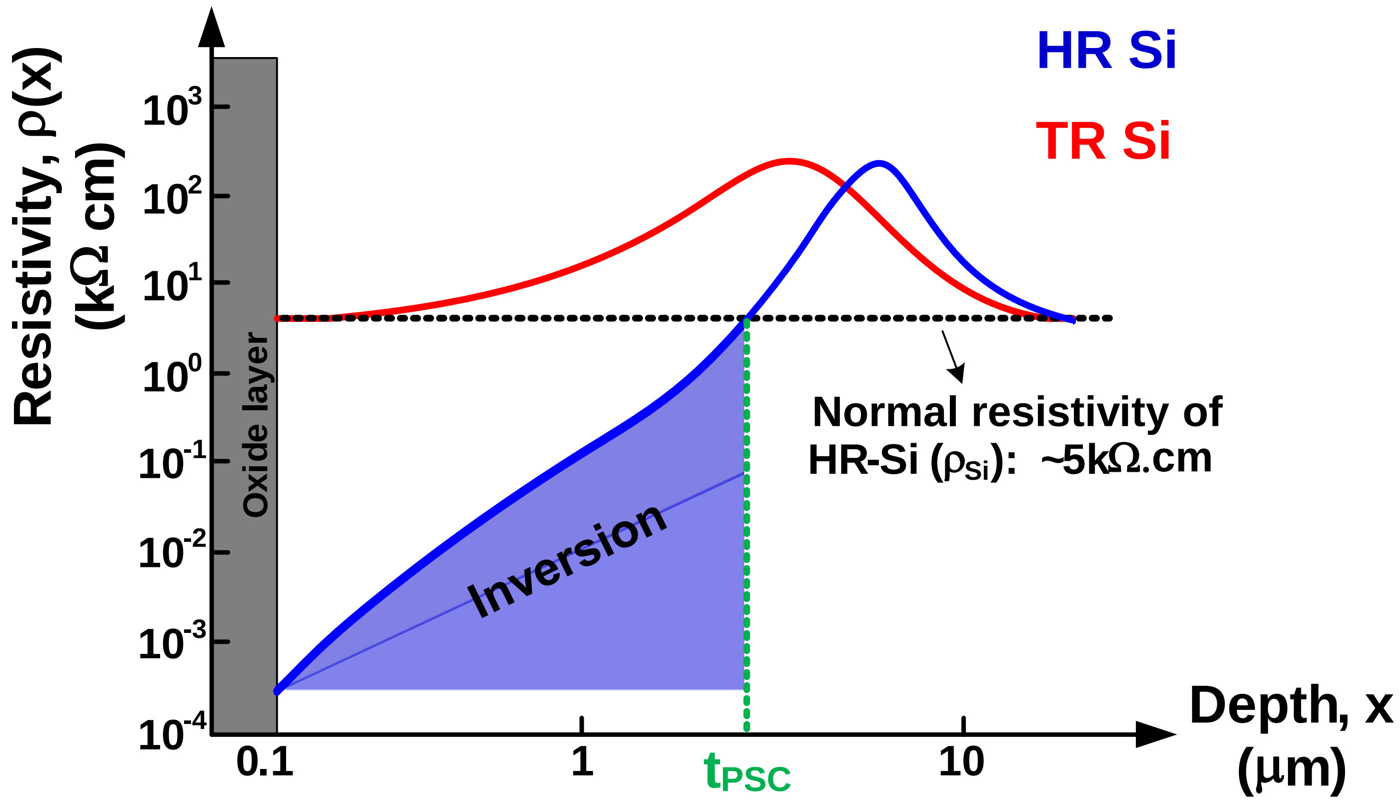
Resistivity vs. Si depth



Nominal resistivity: 5 kΩ.cm (p-type)

Fixed oxide charges: $Q_{ox} = 1 \times 10^{11}$ #/cm^2

Resistivity vs. Si depth



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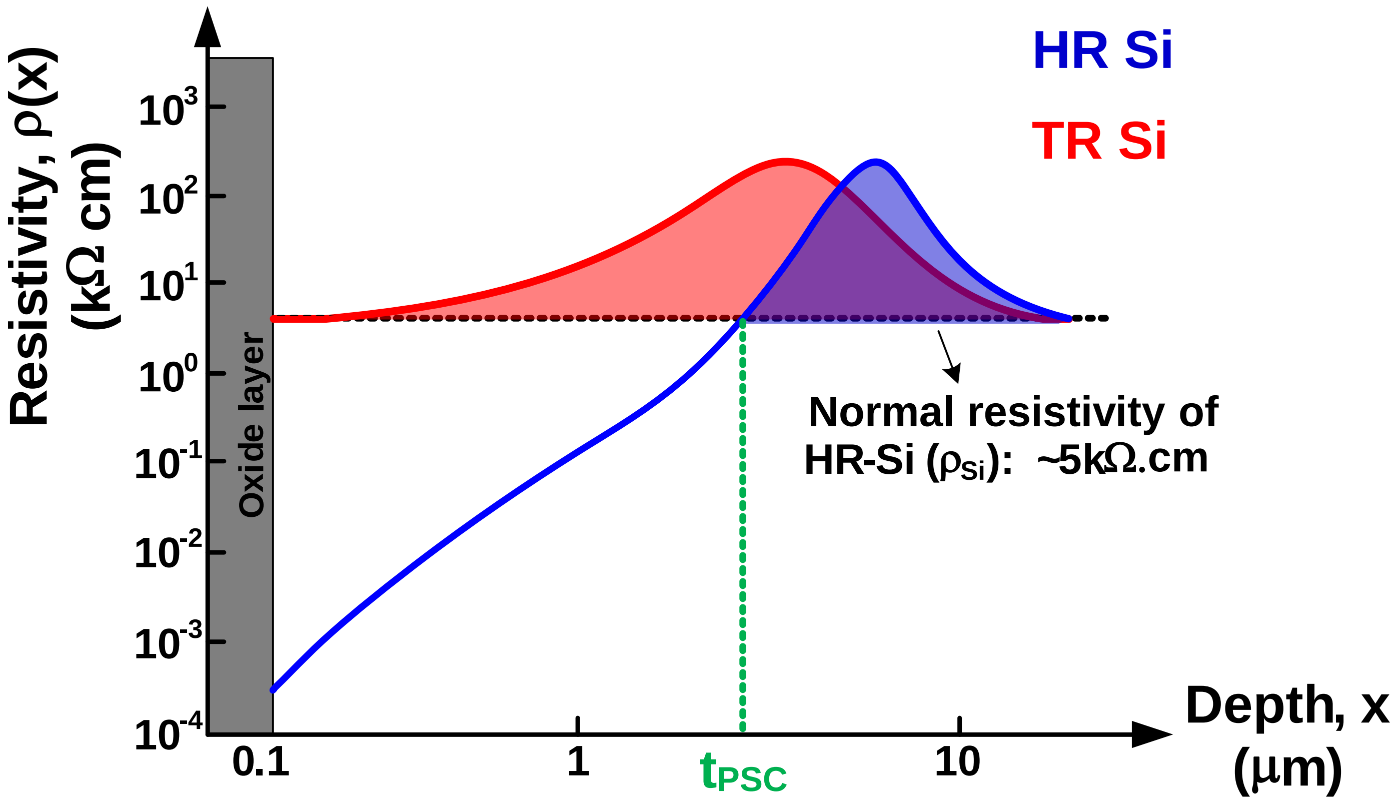
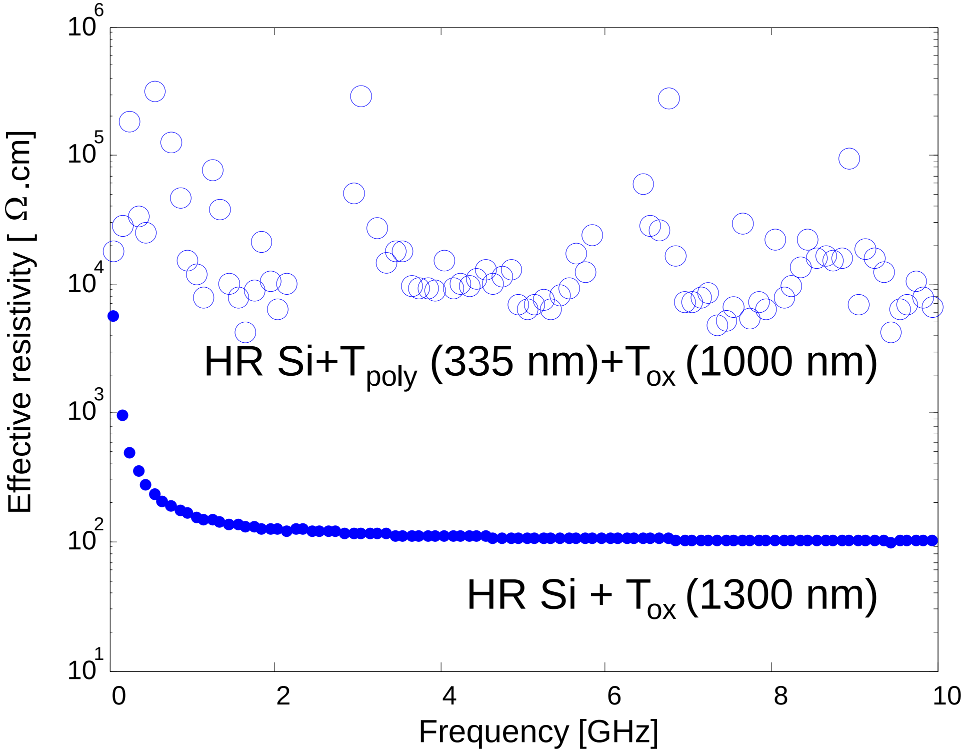


Nominal resistivity: 5 kΩ.cm (p-type)

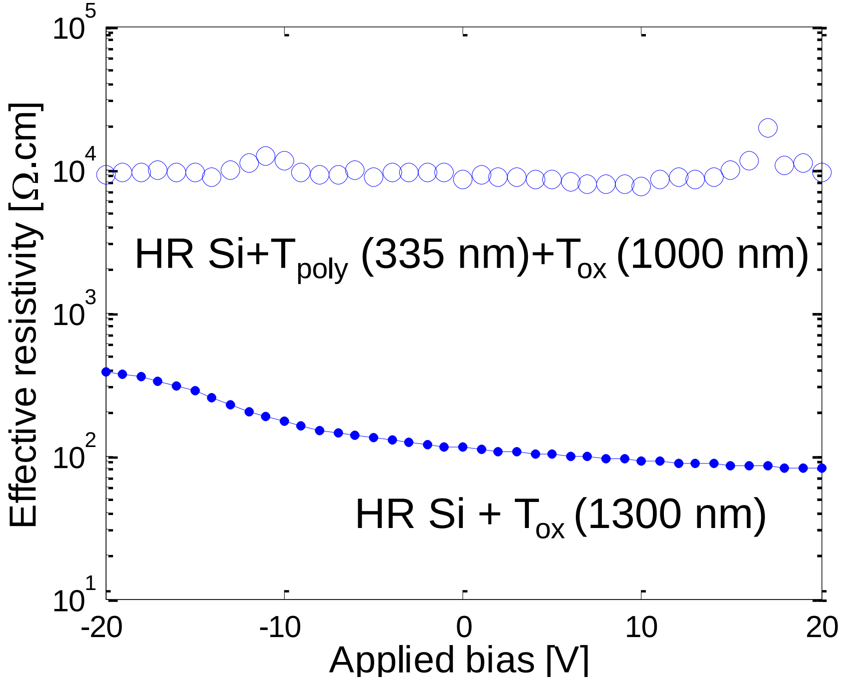
Fixed oxide charges: $Q_{ox} = 1{\times}10^{11}$ #/cm^2

Benefits from passivation

Effective resistivity of CPW: ~10 kΩ.cm



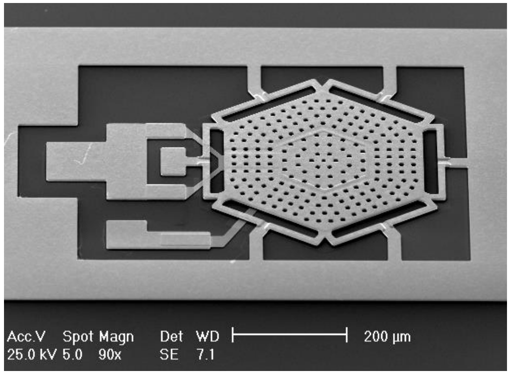
No variation with DC

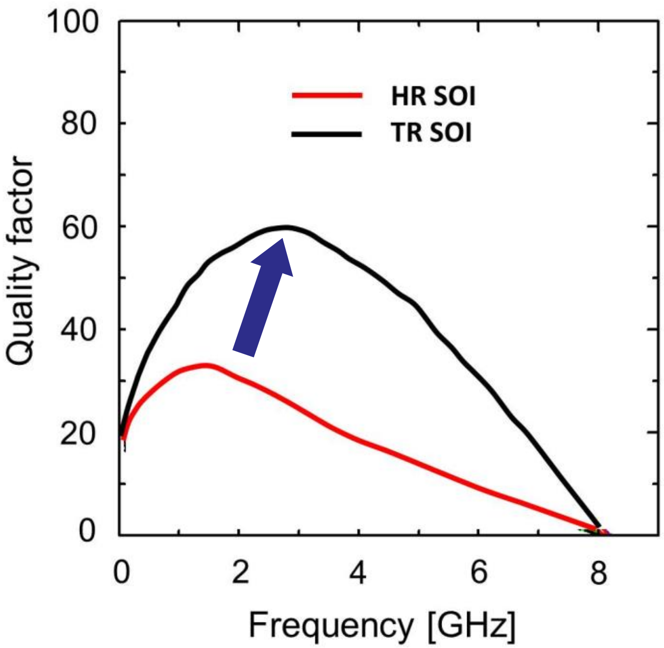


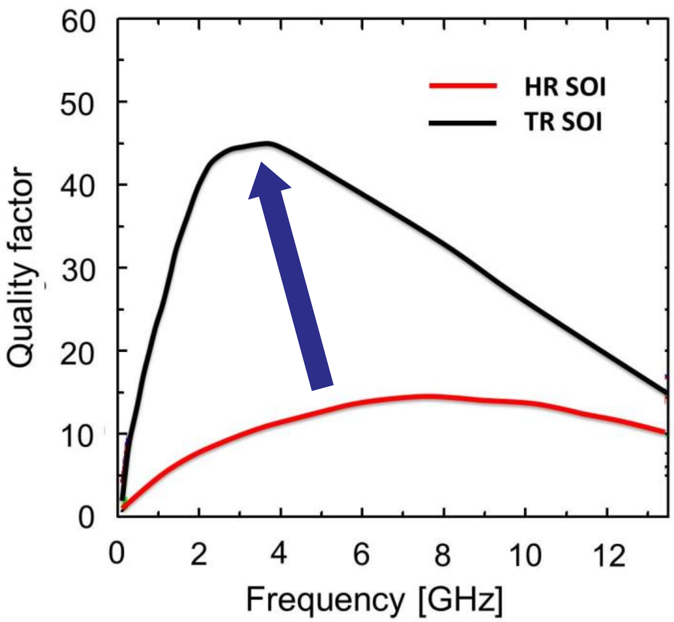
ρ_{nom} > 3 kΩ.cm

[D. Lederer, J.-P. Raskin, *IEEE EDL'05*]

Integrated passive elements







2 nH spiral inductor integrated on top of HR SOI and TR SOI substrates – Cu wire of 35 µm-thick.

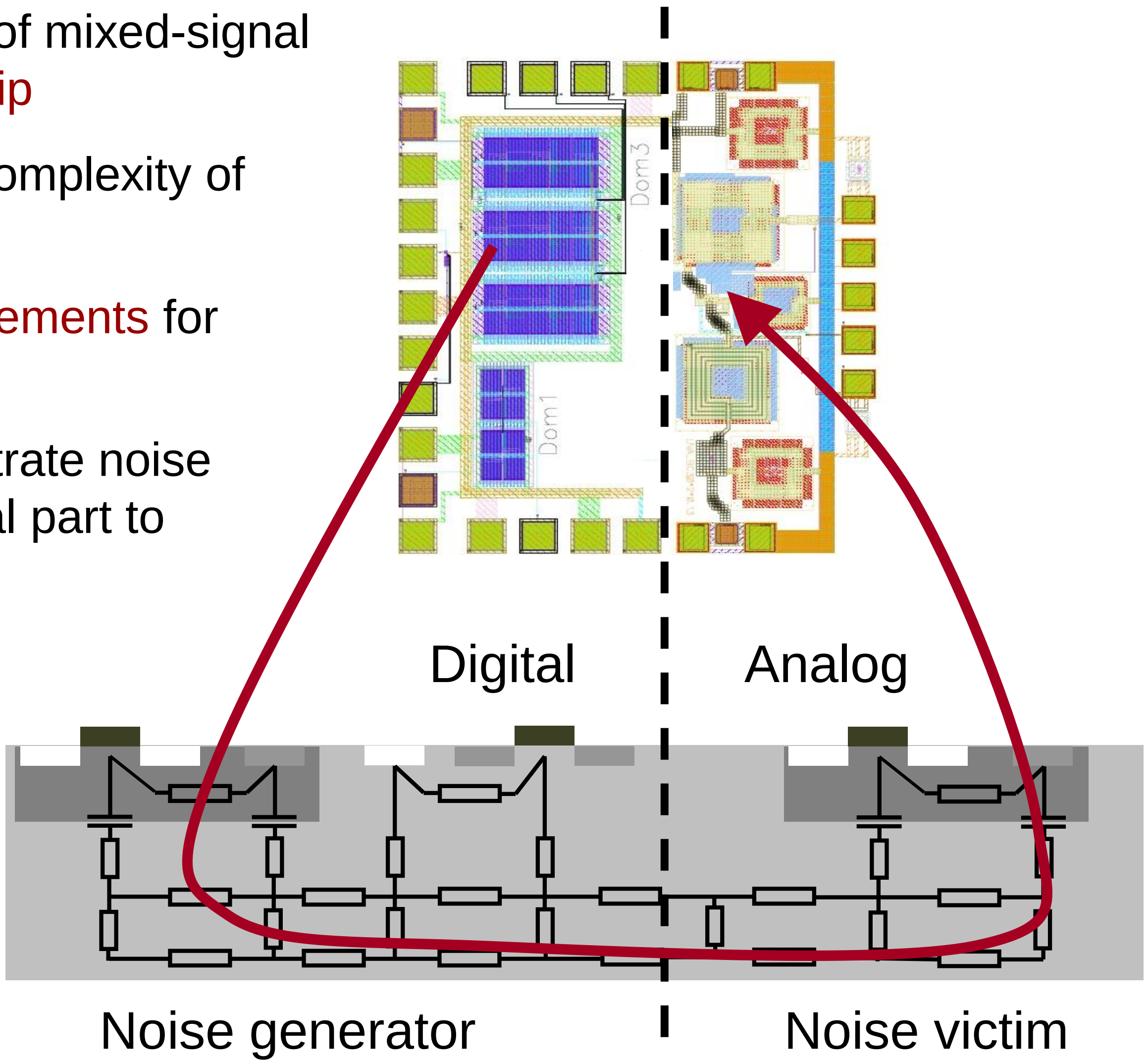
Tunable MEMS capacitor (0.3 – 1.6 pF) integrated on top of HR SOI and TR SOI substrates.

[Yonghyun Shim, J.-P. Raskin, C. Roda Neve, and M. Rais-Zadeh, *IEEE MWCL,* 2013]

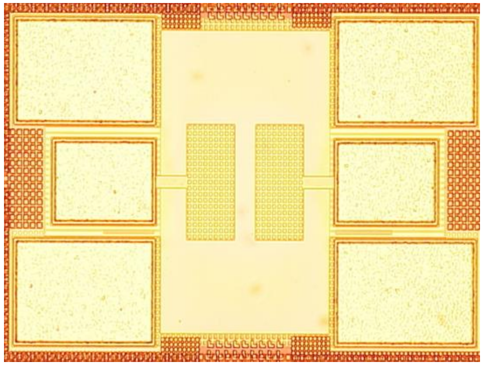
Digital substrate noise

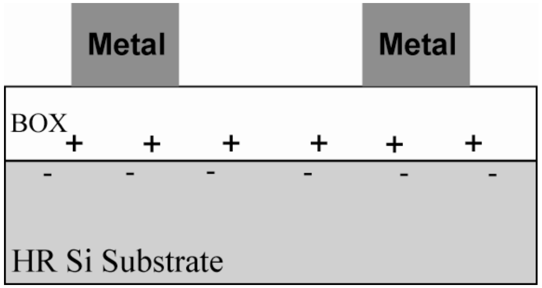
- Rising integration level of mixed-signal circuits onto the same chip
- Increasing speed and complexity of digital circuits
- Higher resolution requirements for analog circuits

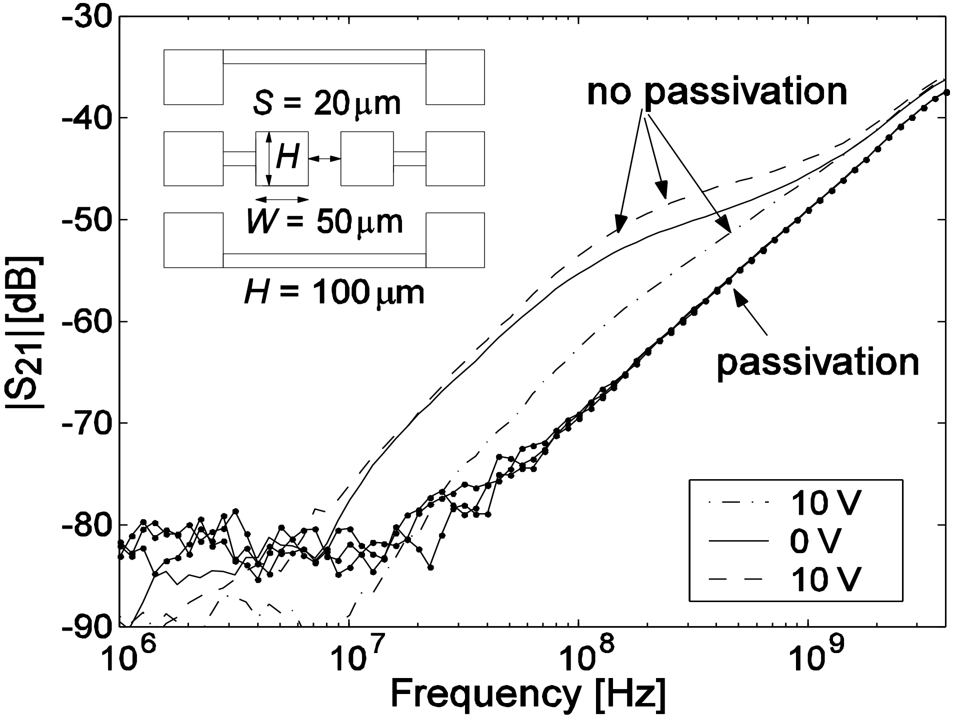
$\Rightarrow$ Higher impact of substrate noise coupling from noisy digital part to sensitive analog part



Crosstalk vs frequency and DC bias







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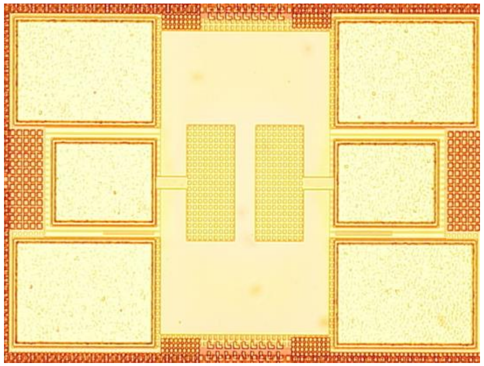
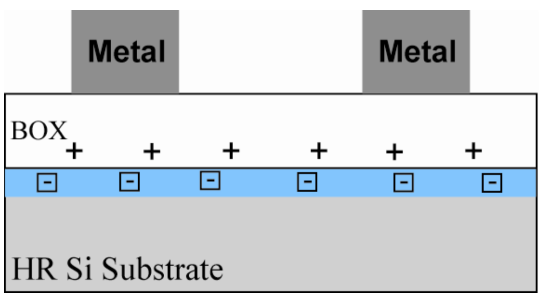
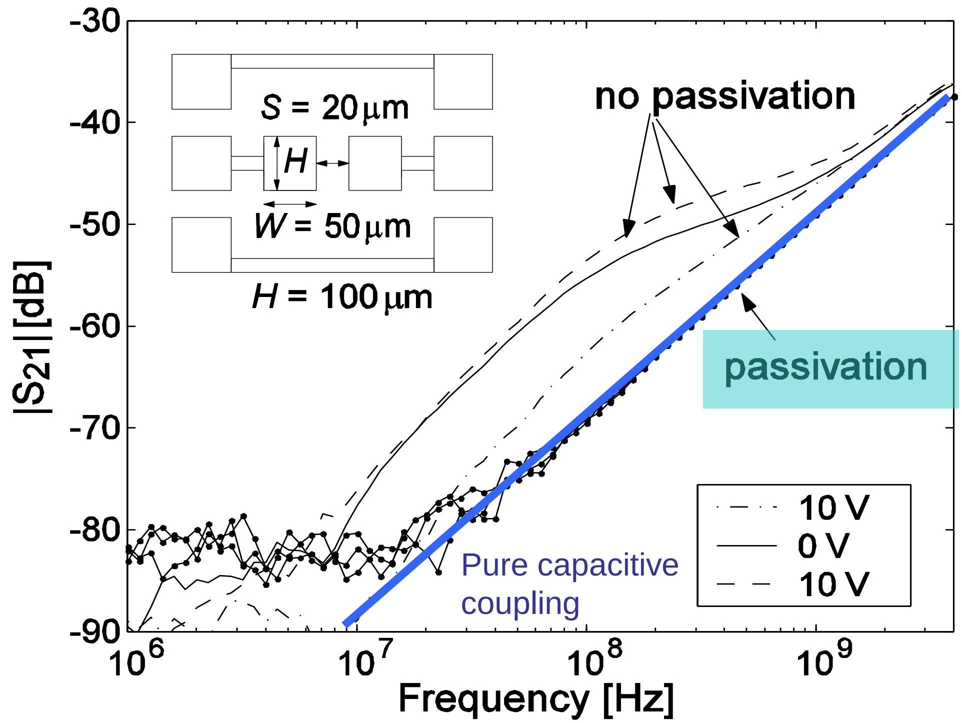






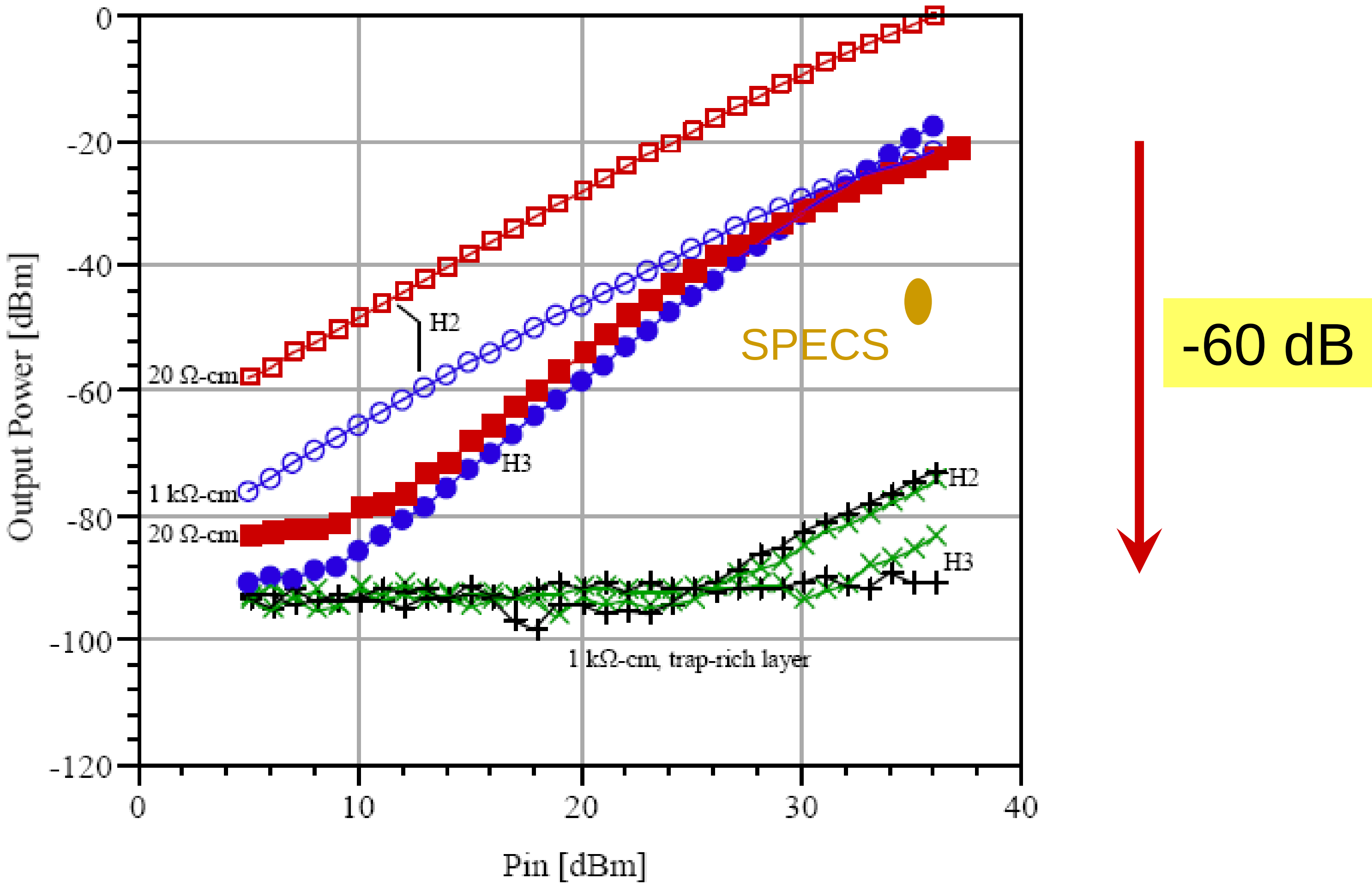
With passivation (poly) layer underneath the BOX: pure capacitive coupling

[D. Lederer, J-P Raskin, *SSE'03*]
[D. Lederer, J-P Raskin, *SSE'05*]
[D. Lederer, J.-P. Raskin, *IEEE EDL'05*]
[K. Ben Ali, J.-P. Raskin, *IEEE TED'12*]

Non-linearities along CPW lines

Integration of many different frequency tones

→ urgent need for **highly linear devices**



[D. Kerr, C. Roda Neve, J.-P. Raskin, *SiRF'08*]

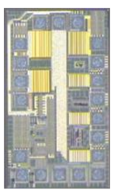
[C. Roda Neve, J.-P. Raskin, *IEEE TED'13*]

RF-SOI substrate has a long history

1992

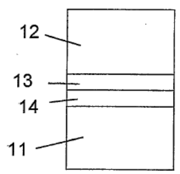
- **Soitec Smart Cut™ SOI**
- **UCL R&D work on HR-SOI**

2003



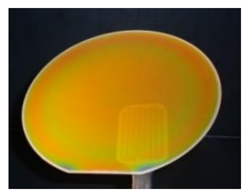
RF switch demo on **HR-SOI**

2005



Trap Rich SOI by UCL and Soitec

2009



- Bonded **Silicon-on-Sapphire** by Soitec & Peregrine

2011

- HR-SOI High Volume Manufacturing
- **eSI™ ramp**

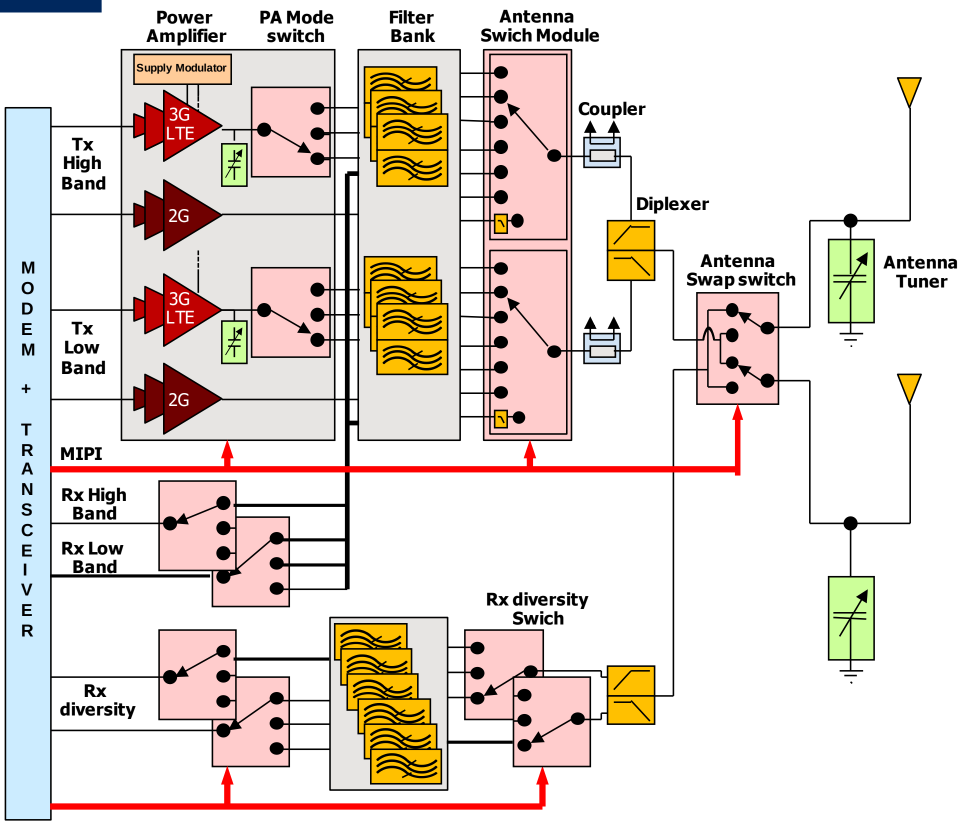
2012

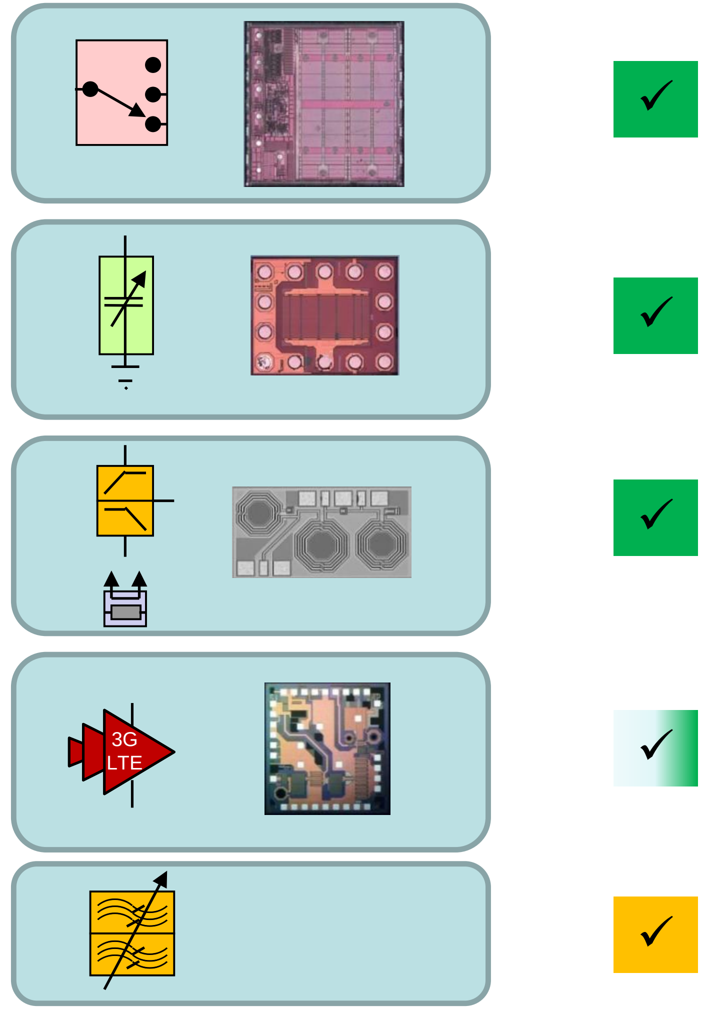
RF switch on **SOI** becomes industry **mainstream**

2014

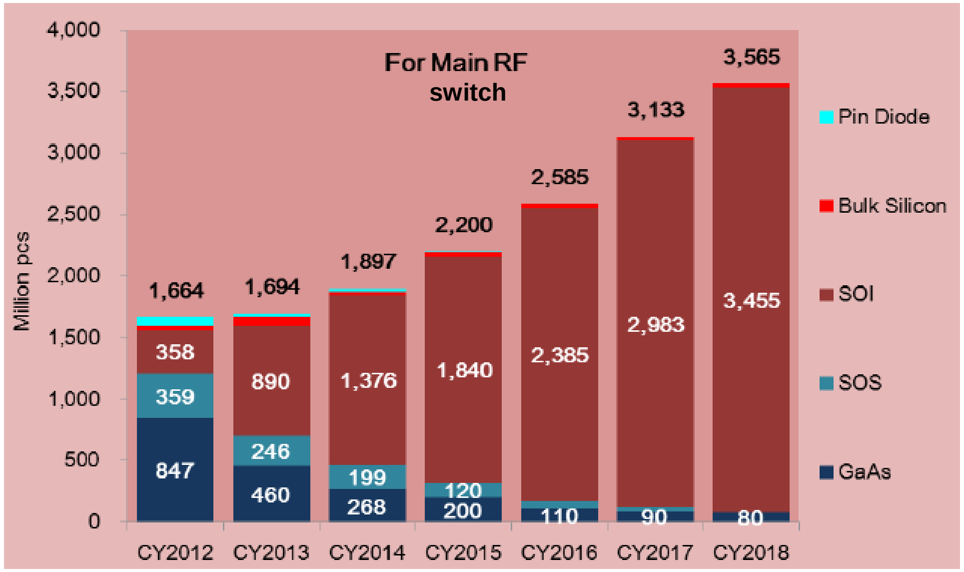
Power Amplifier on RF-SOI ramp

RF-SOI enables Full Front End module integration

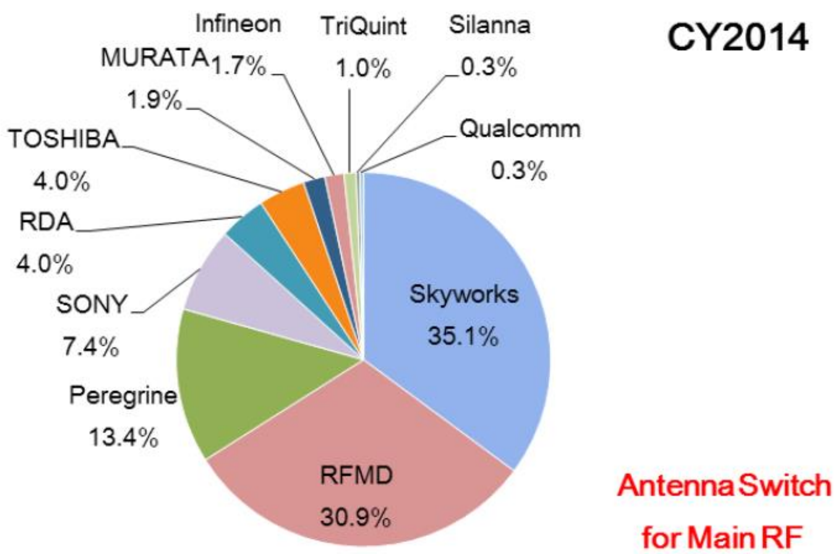




RF-SOI full adoption
In 100% of the SmartPhone - Worldwide foundry offering



Source: Navian, Dec 2014

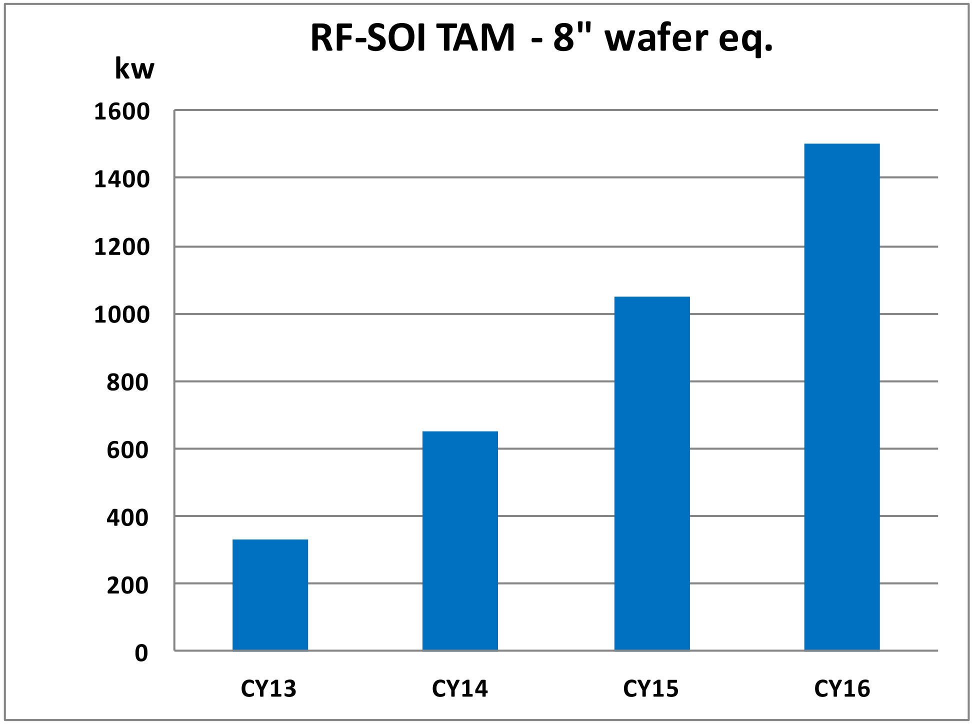


Source: Navian, Dec 2014

GLOBALFOUNDRIES IBM TOWERJAZZ tsmc ST SONY …

More than 15 foundries, Soitec estimates

RF-SOI wafer market more than double every two years
1 millions wafers in 2015



Soitec Estimates

Growth driven by:

- Phone market: 7% CAGR with 630Mu LTE Smartphone
- # used bands: +40% vs CY14
- Power Amplifier integration

Conclusions

- SOI CMOS transistors present **excellent RF performance;**
- **New generation of HR SOI (eSI)** presents outstanding RF performance.

Don't forget, problem might actually turns to solution in another context

Defects, surface states = degradation of MOSFET (↓ μ, ↓ I, ↓ speed, ↓ f_T, …)

But elegant and cheap solution for **HR Si/SOI substrates**

When defects become beauty…

RF SOI – a success story

Acknowledgements

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