"Compact On-Wafer Test Structures for Device RF Characterization"

Kazemi Esfeh, Babak ; Ben Ali, Khaled ; Raskin, Jean-Pierre

Abstract
The main objective of this paper is to validate the radio frequency (RF) characterization procedure based on compact test structures compatible with 50-μm-pitch RF probes. It is shown that by using these new test structures, the layout geometry and hence the on-chip space consumption for complete sets of passive and active devices, e.g., coplanar waveguide transmission lines and RF MOSFETs, is divided by a factor of two. The validity domain of these new compact test structures is demonstrated by comparing their measurement results with classical test structures compatible with 100–150 μm-pitch RF probes. 50-μm-pitch de-embedding structures have been implemented on 0.18-μm RF silicon-on-insulator (SOI) technology. Cutoff frequencies and parasitic elements of the RF SOI transistors are extracted and the RF performance of traprich SOI substrates is analyzed under small- and largesignal conditions.

Document type: Article de périodique (Journal article)

Référence bibliographique

DOI : 10.1109/TED.2017.2717196
Abstract — The main objective of this paper is to validate the radio frequency (RF) characterization procedure based on compact test structures compatible with 50-µm-pitch RF probes. It is shown that by using these new test structures, the layout geometry and hence the on-chip space consumption for complete sets of passive and active devices, e.g., coplanar waveguide transmission lines and RF MOSFETs, is divided by a factor of two. The validity domain of these new compact test structures is demonstrated by comparing their measurement results with classical test structures compatible with 100–150 µm-pitch RF probes. 50-µm-pitch de-embedding structures have been implemented on 0.18-µm RF silicon-on-insulator (SOI) technology. Cutoff frequencies and parasitic elements of the RF SOI transistors are extracted and the RF performance of trap-rich SOI substrates is analyzed under small- and large-signal conditions.

Index Terms — 50-µm-pitch RF probes, coplanar waveguide (CPW) transmission lines, on-wafer RF characterization, RF MOSFET parasitic extraction, RF pads, RF test structures, silicon-on-insulator (SOI) technology, trap-rich high-resistivity SOI substrate.

I. INTRODUCTION

IN RECENT years, a high degree of miniaturization of CMOS technology provided the opportunity of developing integrated circuits operating in the gigahertz range and also low-cost high-level integration analog, digital, and radio frequency (RF) functions on the same wafer for system-on-chip or in system-in-package applications [1]–[6]. The amazing multiplication of analog/RF applications in CMOS technologies leads to an increased interest of routinely characterizing the analog and RF performance of newly developed technological nodes. Classically, test structures such as battery of transistors with various geometries and dimensions, capacitors array, and contacts chain are embedded with metallic pads usually named dc pads which are probed by simple metallic needles. Due to the poor propagation of ac signal along classical metallic needles, the frequency analysis of the device under test (DUT) is limited to a maximum of a few megahertz. In order to perform on-wafer characterization of DUT over a wide frequency band up to a few tens of gigahertz, the RF signal integrity must be conserved from the signal generator output up to the on-chip input of the DUT. To do so, DUT must be embedded in well-designed coplanar waveguide (CPW) feed lines and pads [7]. RF CPW pads with a pitch, distance between the central conductor and the planar lateral ground, of 100 or 150 µm are currently used in the industry. Those RF CPW pads dimensions are quite important compared with the size of the DUT itself. Therefore, because of the large footprint and thus the related cost issues of the RF test structures, none or only a few RF DUTs are characterized at the early stage of development of new technological nodes. Without access to a sufficient number of RF test structures, RF models for transistors, passive elements, and substrate cannot be properly developed and no feedback can be provided to fabrication process engineers for optimizing the technology for dedicated RF applications. Then, it is of first importance to reduce as much as we can the layout dimensions of the RF test structures and multiply the presence of those on mask sets used for qualifying a new technological node.

Recently, 50-µm-pitch RF probes are available on the market providing the opportunity to perform on-wafer wideband characterization with more compact test structures. To the best knowledge of the authors, there is no validation of the 50-µm-pitch RF probes to fully characterize the RF performance of passive and active devices in CMOS technology. Scaling down the RF probes dimensions and thus reducing the spacing between the central and ground RF pads could lead to, respectively, a larger contact resistance and parasitic RF pad capacitances, thus degrading the accuracy of the de-embedding procedure. In this paper, we design de-embedding test structures and battery of passive and active devices to demonstrate the validity of these new compact RF pads. All the experiments presented hereafter are made in 0.18-µm-RF silicon-on-insulator (SOI) technology. We chose RF SOI since it is today a mainstream technology for any low-power wireless applications. The commercial success of RF SOI is explained by the ICs low-power consumption [8], [9], its high immunity to crosstalk in mixed-signal RF ICs [10], [11], and the high linearity of the RF functionalities integrated on trap-rich high-resistivity (HR) SOI substrate [12], [13]. RF switches which were mostly designed in GaAs technology four years ago are today, for more than 95% of them, integrated in RF SOI [1], [14]. Scattering (S-) parameters measured with a vectorial network analyzer from 10 MHz
up to 26.5 GHz are made for DUTs embedded between RF pads compatible with classical CPW probes characterized by a pitch of 100 or 150 µm and compared with test structures designed for 50-µm-pitch probes. Cutoff frequencies and parasitic elements of the RF SOI transistors are extracted and the RF performance of trap-rich SOI substrates is analyzed under small- and large-signal conditions using the different RF probes and pads dimensions. It is demonstrated that 50-µm-pitch probing provides reliable microwave characterization, drastically reduces the RF test structures footprint without increasing the parasitic capacitances associated with RF CPW pads.

II. DEVICES DESCRIPTION

In this paper, the test structures, i.e., CPW transmission lines and RF MOSFETs are fabricated using TowerJazz 0.18 µm, four-metal layer SOI CMOS process on top of second-generation (RFeSi90) trap-rich HR-SOI UNIBOND wafers provided by SOITEC and having a 200-nm-thick BOX and a handle Si substrate resistivity of around 8 kΩ·cm (Fig. 1). The devices under test are described in detail hereafter.

A. Coplanar Waveguide Transmission Lines

Three sets of CPW line test structures are designed and named CPW Set 1, CPW Set 2, and CPW Set 3, compatible with RF probe pitches from 50–150, 50–100, and only 50 µm, respectively. Each set includes 2100-, 1500-, and 1000-µm-long CPW lines with 0.52-µm-thick aluminum and dimensions of, respectively, 20 and 18 µm for the central conductor (W) and slot space (S).

Dedicated de-embedding structures such as open (with a pads distance of 90 µm), short, and thru are included in each set as well. The ground plane of CPW lines in CPW Set 1, 2, and 3 has a width of 172, 100, and 60 µm, respectively. Each set includes 2100-, 1500-, and 1000-µm-long CPW lines with 0.52-µm-thick aluminum and dimensions of, respectively, 20 and 18 µm for the central conductor (W) and slot space (S).

As can be seen in Fig. 2, by moving from CPW Set 1 to CPW Set 2 and CPW Set 3, 33% and 53% of space saving is achievable, respectively. In this paper, the longest CPW lines of 2,100 µm in CPW Set 1 to CPW Set 3 are used to extract the effective permittivity and resistivity of the substrate since they are the most sensitive ones and thus lead to a more accurate comparison between the classical RF pads and the 50-µm-pitch ones.

B. RF MOSFETs

The body-tied partially depleted (PD) SOI nMOSFETs have 145 nm of thin active silicon film with a nominal operating voltage of 2.5 V. The studied RF MOSFETs have five different gate lengths (Lg) ranging from 240 to 320 nm with a total gate width of 32 µm including 16 gate fingers of 2 µm each (Wf). For RF characterization and comparison three types of CPW feed lines and RF pads compatible with 150-µm (MOS Set 1), 50–150-µm (MOS Set 2), and 50-µm pitch (MOS Set 3) are embedded to the multifinger device, as shown in Fig. 3. For each set of nMOSFETs, dedicated open and short de-embedding structures are provided to eliminate the parasitic effect of the feed lines and RF pads using open-short de-embedding method.

As can be seen in Fig. 3, the RF MOSFETs’ test structures compatible with 50-µm pitch in MOS Set 3 takes almost 47% less layout space than the battery of transistors embedded with the classical RF pads (MOS Set 1).

III. MEASUREMENT DESCRIPTION AND RESULTS

A. CPW Transmission Lines

On-wafer small-signal measurements of the longest CPW line (line A) of each set characterized by different RF pad pitches as shown in Fig. 2 were carried out and compared. The RF S-parameters measurements are performed by using an Agilent N5242A in the frequency range between 10 MHz and 26.5 GHz. The reference planes at the probe tips are determined by the off-wafer line-reflect-reflect-match (LRRM) calibration using a commercially available calibration kit from Cascade. From the measured S-parameters, the RF pads are de-embedded using the thru-reflect-line method described.

Fig. 1. Cross section details of four-metal layer 0.18-µm-SOI CMOS process by TowerJazz on top of second-generation (RFeSi90) trap-rich high-resistivity SOI substrate provided by SOITEC.

Fig. 2. CPW lines details for (a) CPW Set 1 (compatible with 50–150 µm pitch), (b) CPW Set 2 (compatible with 50–100 µm pitch), and (c) CPW Set 3 (compatible with 50-µm pitch).

Fig. 3. RF MOSFETs’ test structures compatible with 50-µm pitch in MOS Set 3 takes almost 47% less layout space than the battery of transistors embedded with the classical RF pads (MOS Set 1).
Fig. 3. RF PD SOI MOSFETs compatible with (a) 150-µm pitch (MOS Set1), (b) 50–150-µm pitch (MOS Set2), and (c) 50-µm pitch (MOS Set3) RF probes.

in [7], and the RF insertion losses ($\alpha$) and the characteristic impedances are shown in Fig. 4(a) and (b), respectively. Applying the extraction method proposed in [15] on the de-embedded S-parameters, the substrate effective resistivity ($\rho_{\text{eff}}$), and effective permittivity ($\varepsilon_{\text{eff}}$) are extracted and presented in Fig. 4(c) and (d), respectively. As can be seen in Fig. 4, the extracted parameters of CPW lines lying on SOI substrate for the three sets of CPW lines using different probe pitches are quite similar. Moreover, from Fig. 4(c) we can see that the extracted substrate effective resistivity up to 5 GHz is higher than 1 kΩ·cm as expected for trap-rich high-resistivity SOI substrates, whereas this parameter for classical HR-SOI is reported to be only about 200 Ω·cm [16].

Based on a four-port Agilent PNA-X vector network analyzer [17], the nonlinear behavior of the substrate is measured using a one-tone characterization setup [18]. By applying an input signal varying from $-25$ up to 25 dBm at 900 MHz the second (H2) and third harmonic (H3) components are measured at the output port of the CPW line at 0 V bias. The measurement is performed using Z- and infinity-RF probes on three different sets of designed CPW lines shown in Fig. 2. As can be seen in Fig. 5, all measurements show similar results ($H2 \sim -65$ dBm and $H3 \sim -78$ dBm at 25 dBm fundamental tone output power) for the line A of the different sets compatible with different RF pads pitches. A slightly difference observed in H3 between Z- and infinity-probes can be explained by different contact quality.

From these experimental results we can clearly conclude that the small- and large-signal substrate characteristics can be properly extracted using CPW lines embedded in 50-µm-pitch RF pads, thus drastically minimize the footprint of the needed RF structures, and then the cost related to the technology assessment and monitoring.

Fig. 4. Comparison of four different parameters of the studied RFeSi90 substrate using different probe types and pitches. (a) Total insertion losses (conductor + substrate), (b) Lines characteristic impedance, (c) Effective resistivity, (d) Effective permittivity extracted from CPW Set 1, CPW Set 2, and CPW Set 3 using line A after open-thru de-embedding.
S-parameters curves for all types of test structures, namely, methods in the literature [23]–[26]. The extraction method of MOSFET. All the intrinsic elements are contained in the light blue box.

B. Body-Tied Partially Depleted SOI nMOSFET

RF and dc on-wafer measurements have been done using an Agilent N5242A for high-frequency S-parameters measurement from 10 MHz to 26.5 GHz in combination with HP4145A semiconductor parameter analyzer for extracting the static parameters, e.g., threshold voltage ($V_{th}$), drain induced barrier lowering, transconductance, early voltage, etc. The reference planes at the probe tips are determined by the off-wafer LRRM calibration using a commercially available calibration kit from Cascade. From the measured S-parameters, the RF pads are de-embedded by using the open-short method [19]. Based on the MOSFET small-signal equivalent circuit presented in Fig. 6, by means of ac analysis all parasitic elements and RF figures of merit, e.g., $f_T$ (current cutoff frequency) and $f_{max}$ (maximum oscillation frequency) are extracted [20]–[22]. The extraction of parasitic elements shown in Fig. 6 including series resistances ($R_s$, $R_{ds}$, and $R_g$) and inductances ($L_s$, $L_d$, and $L_g$), intrinsic and extrinsic capacitances ($C_{ds}$, $C_{gs}$, and $C_{gd}$ denoted by “t” and “e,” respectively), and intrinsic transconductance ($g_m$) and output conductance ($g_{ds}$) were proposed and reported by different methods in the literature [23]–[26]. The extraction method of $f_T$ and $f_{max}$, the two most important RF figures of merit for transistors, is well studied and reported [27]–[30].

In this paper, the parasitic elements and the cutoff frequencies of PD SOI nMOSFETs are extracted from the S-parameters measured with two types of embedded RF pads, i.e., 50- and 150-μm pitch, as shown in Fig. 3, and they are compared. The S-parameters measurement results in saturation regime ($V_{ds} = 1.2$ V and $V_{gs}$ at which $g_m$ is maximum) are presented in Fig. 7 and show a good agreement between S-parameters curves for all types of test structures, namely, MOS Set 1, MOS Set 2, and MOS Set 3, compatible with 150-, 50–150-, and 50-μm pitch, respectively.

A gate length $L_{NOM}$ close to the minimum allowed for standard logic in this technology was used for the following evaluation. As shown in Fig. 7, a good matching between all the small-signal extracted parameters obtained with two types of RF pads is demonstrated, then validating the 50-μm-pitch probing. As shown in Fig. 7, for a MOSFET of this gate length extrinsic $f_T$ and $f_{max}$ of 26 and 50 GHz is achieved, respectively. Intrinsic ($g_m$) and extrinsic ($g_{me}$) derivatives of the transfer characteristic ($I_{ds} - V_{gs}$), at $V_{ds} = 1.2$ V and $V_{gs}$ at which $g_{me}$ is maximum, of 421 and 381 mS/mm are extracted [Fig. 7(b)]. These parameters are in very good agreement with the benchmarking of $f_T$ and $g_{me}$ for PD-SOI technology [21], [28] and International Technology Roadmap for Semiconductor [2]. In Fig. 8(c) one can observe that the major part of total gate capacitance in saturation, i.e., $C_{gTot}$ = $C_{gTot} + C_{gDots}$ is coming from gate–source capacitance $C_{gTot}$ as expected for this channel length. The total source–drain capacitance ($C_{dsTot}$) which is mainly affected by substrate shows quite low value in SOI technology especially in trap–rich HR-SOI compared with other technologies like bulk [31] even though in this paper the BOX thickness is 200 nm whereas it is 1 μm in the case of conventional HR SOI substrates.

To investigate the relative importance of the RF pads embedded to the transistor under test, the S-parameters of the open structures associated with the transistor shown in Fig. 3 are measured. Based on the capacitance network of open structure shown in the inset of Fig. 9, by using Y-parameters, the input, and transferred capacitances, respectively, denoted by $C_{11}$ and $C_{12}$ can be expressed as

$$C_{11} = \frac{\text{Im}(Y_{11}) + Y_{12}}{2\pi f}$$

(1)

$$C_{12} = \frac{-\text{Im}(Y_{12})}{2\pi f}$$

(2)

The extracted capacitances $C_{11}$ and $C_{12}$ for three types of RF pads compatible with 150-, 50–150-, and 50-μm pitch, respectively, are illustrated in Fig. 9. The transfer capacitance $C_{12}$ is composed of two parallel capacitors, one representing
KAZEMI ESFEH et al.: COMPACT ON-WAVER TEST STRUCTURES 3105

Fig. 8. Comparison of different extracted small-signal equivalent circuit lumped elements and RF figures of merit of the PD SOI nMOSFET having 16 fingers ($N_f$) of 2-µm width ($W_f$) each compatible with 50-and 150-µm pitch. (a) RF figures of merit ($f_T$ and $f_{max}$). (b) Intrinsic ($g_{mi}$), extrinsic ($g_{me}$) transconductance, and channel output conductance ($g_{ds}$). (c) Total source–drain ($C_{dstot}$), gate–drain ($C_{gdtot}$), and gate–source ($C_{gstot}$) capacitances. (d) Normalized gate ($R_g$) and source/drain ($R_{sd}$) resistances.

the coupling into the substrate and the other one in the air above the structures.

Thanks to the high-resistivity properties of the trap-rich SOI substrate, $C_{12}$ (crosstalk capacitance) is quite small and around 1 fF for all CPW RF pads. When moving from 150-µm (MOS Set 1) down to 50-µm pitch (MOS Set 3) RF probe the spacing between the central pad and coplanar grounds is reduced which leads to an increase of the parasitic capacitance of the RF pads. But the increment of the RF pads parasitic capacitances is quite limited (around 25%) thanks to the reduction of the RF pads area, from 106.4 to 50.4 µm² for, respectively, the 150- and 50-µm-pitch RF probes. It is worth noting that the absolute parasitic capacitances of the RF pads stay below the RF transistor capacitances and the accurate extraction of lumped elements of the transistor small-signal model with a simple open-short de-embedding method is valid up to a few tens of gigahertz.

Fig. 10 presents the comparison of total gate capacitance ($C_{gstot} = C_{gstot} + C_{gdetot}$) of the measured RF SOI MOSFETs of different gate lengths with parasitic input capacitances ($C_{11}$) of RF pads. From Fig. 10, it can be observed that the parasitic capacitance of both open structures with 150- and 50-µm pitch is below the value of the total gate capacitances in saturation and cold regimes. Moreover, it can be seen that the results of extraction using MOS Set 1 and 3 are well consistent. With the transistor gate shrinkage, it will be more and more important to keep the parasitic lumped elements of the RF pads as low as possible.

As reported in [20], the 25-nm-gate length transistor with a total gate width of 120 µm, shows a total gate capacitance of 90 fF which is still larger than $C_{11}$ associated with 50-µm-pitch RF pads.

IV. CONCLUSION

In this paper, a comparison between characterized passive and active devices on trap-rich SOI substrate by means of different sets of test structures compatible with 150–100-
50-μm-pitch pads is reported. It is shown that in both cases the final results are in good agreement while using the RF test structures compatible with 50-μm pitch, 53% and 47% of die space savings are achieved for CPW transmission lines and nMOSFETs, respectively. Thanks to the footprint reduction of the RF test structures, we can either introduce more RF test structures on a defined area or we can reduce the die area consumed by them and thus diminish the test cost per wafer. It is also shown that the 50-μm-pitch RF pads capacitances are still under control and low enough favoring the accurate characterization of highly scaled-down technological nodes. 50-μm-pitch RF probes will be used for future characterization of advanced MOSFETs presenting cutoff frequencies in millimeter-wave frequency range.

ACKNOWLEDGMENT

The authors would like to thank TowerJazz team for the fabrication of CMOS devices and SOITEC for providing the trap-rich SOI wafers.

REFERENCES


Babak Kazemi Esfeh received the B.S. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1997, the M.S. degree in microwave engineering from Putra University, Selangor, Malaysia, in 2009, and the M.S. degree from Gävle University, Gävle, Sweden, in 2012. He is currently pursuing the Ph.D. degree in wide-band characterization of trap-rich high-resistivity SOI substrates with high resistivity for system-on-a-chip and monolithic microwave integrated circuit applications.
Khaled Ben Ali received the Ph.D. degree in engineering sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 2014. Since 2015, he has been a Senior Researcher with the Université Catholique de Louvain. His current research interests include the characterization of Si-based substrates for RF SOI applications, and LDMOS simulations and characterization for radiation hardness and high temperature space applications.

Jean-Pierre Raskin (M’97–SM’06–F’14) received the M.S. and Ph.D. degrees in applied sciences from the Université Catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1994 and 1997, respectively. He has been a Professor and the Head of the Electrical Engineering Department with UCL, since 2000 and 2014, respectively.